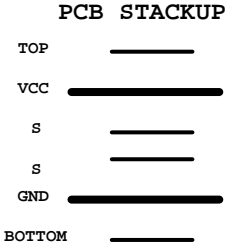


# Cathedral Peak 2A Block Diagram

Project code: 91.4K901.001  
PCB P/N : 48.4K901.001  
REVISION : 08220- -1



SYSTEM DC/DC	
TPS51125	37
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A)
	3D3V_S5(6A)

SYSTEM DC/DC	
RT8202 X 2	38
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A)
	1D2V_S0(4A)

SYSTEM DC/DC	
RT8202	39
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9026PFP	
	39
5V_S5	DDR_VREF_S3
	0D9V_S3

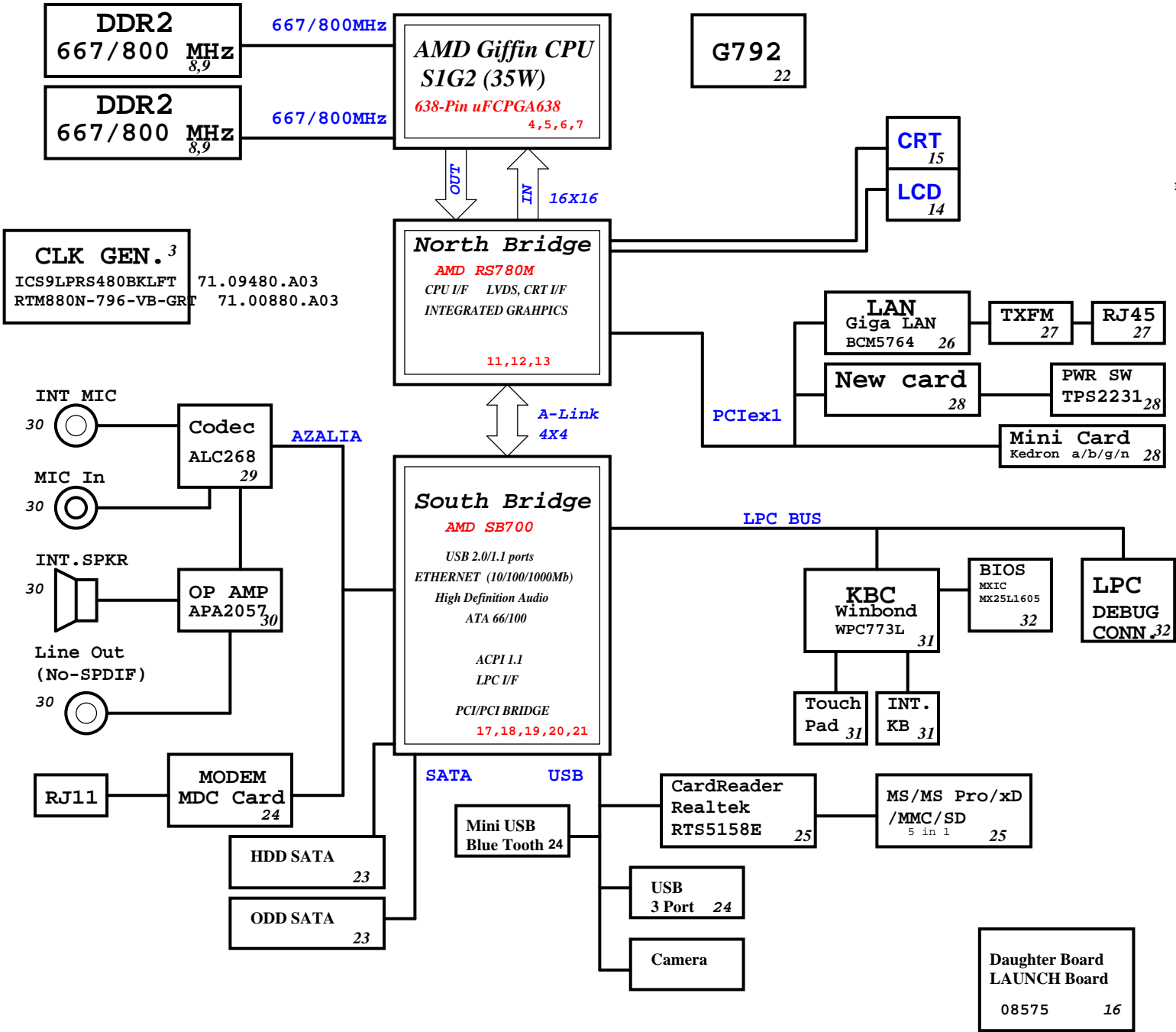
RT9161	
	40
3D3V_S0	2D5V_S0
	(200mA)

G957	
	40
3D3V_S0	1D5V_S0
	(1A)

G9161	
	40
3D3V_S5	1D2V_S5
	(400mA)

CHARGER	
MAX8731	41
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR
	18V 6.0A
	UP+5V
	5V 100mA

CPU DC/DC	
ISL6265HR	36
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0
	0~1.55V 18A
	VCC_CORE_S0_1
	0~1.55V 18A
	VDDNB
	0~1.55V 18A



<Core Design>

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Title

**BLOCK DIAGRAM**

Size A3 Document Number Rev

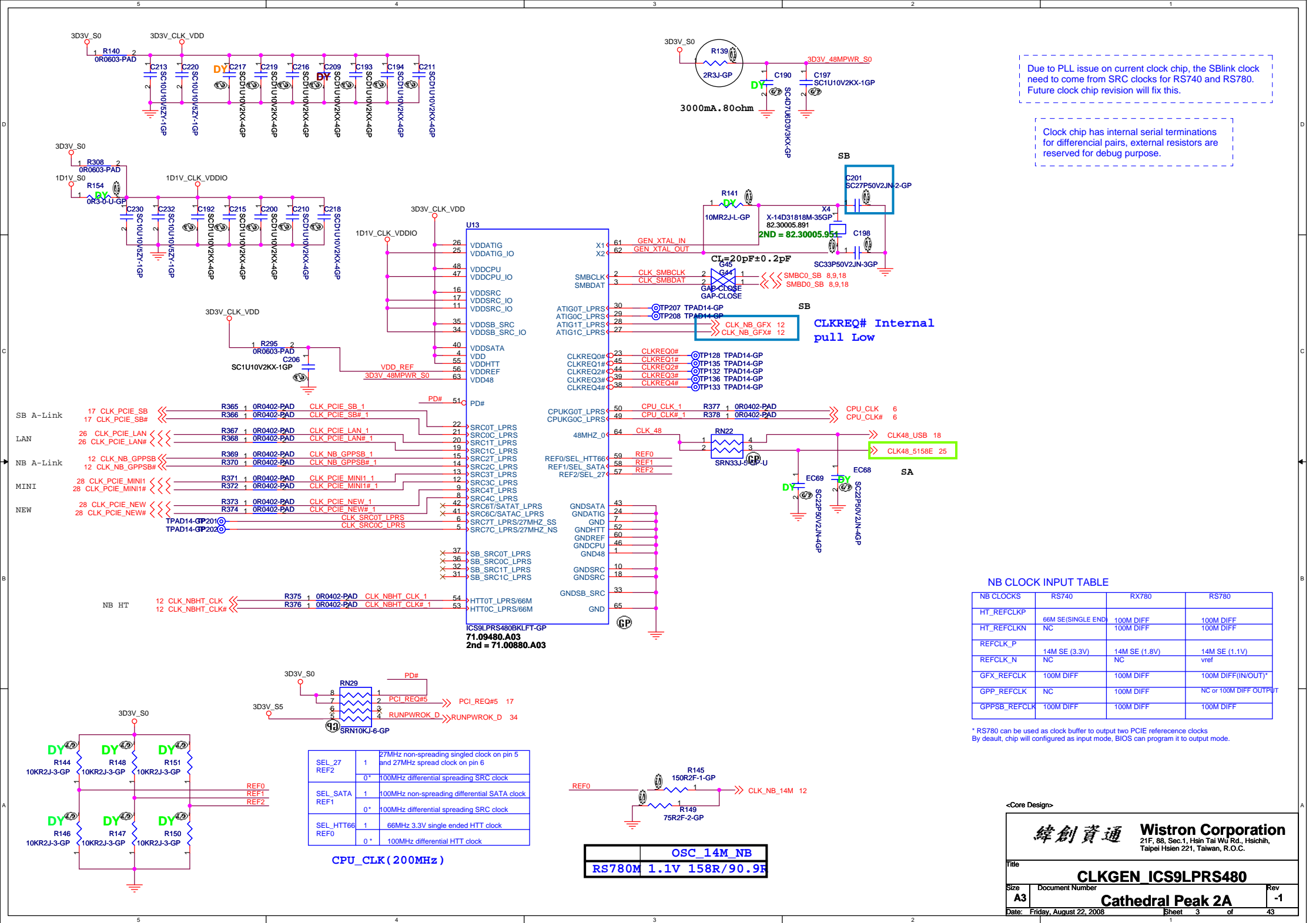
Date: Friday, August 22, 2008 Sheet 1 of 43

**Cathedral Peak 2A**  
-1

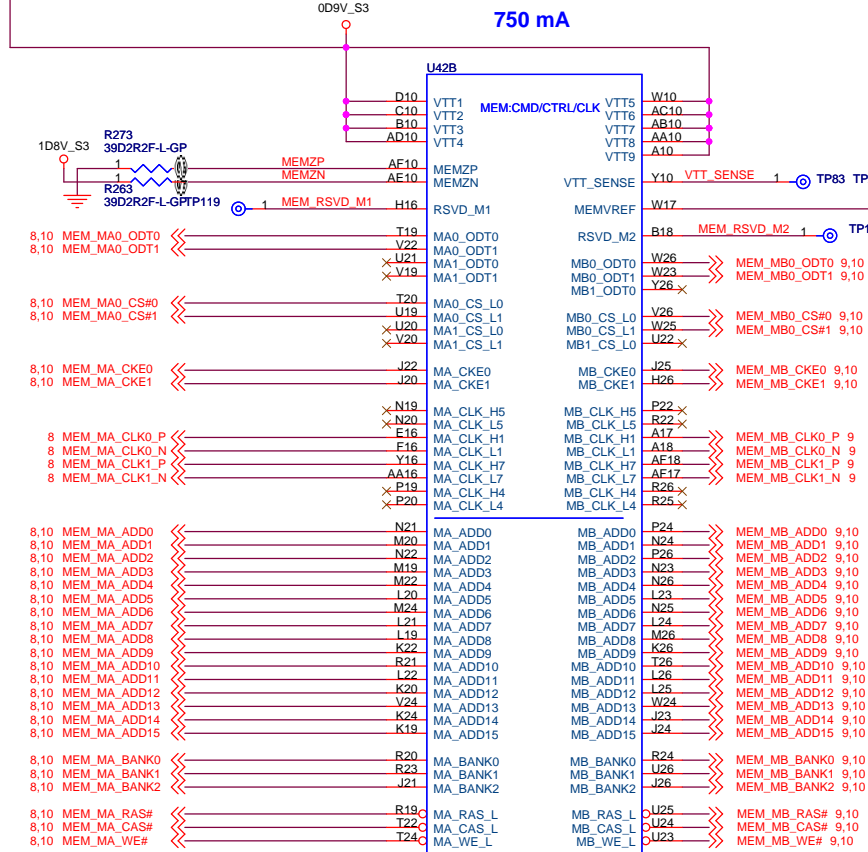
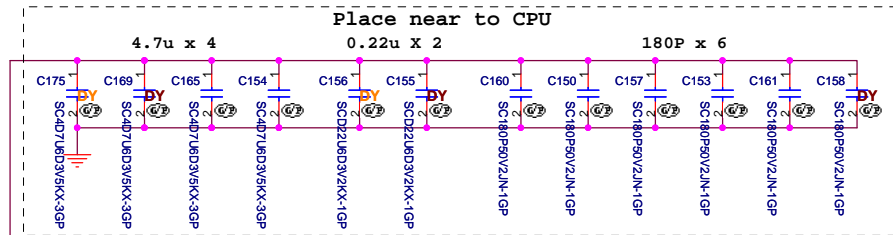
5	4	3	2	1
D				
C				
B				
A				

<Core Design>

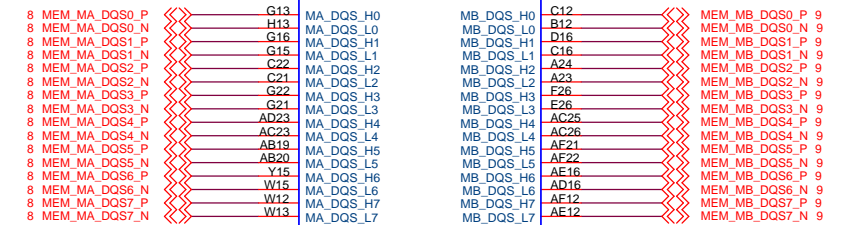
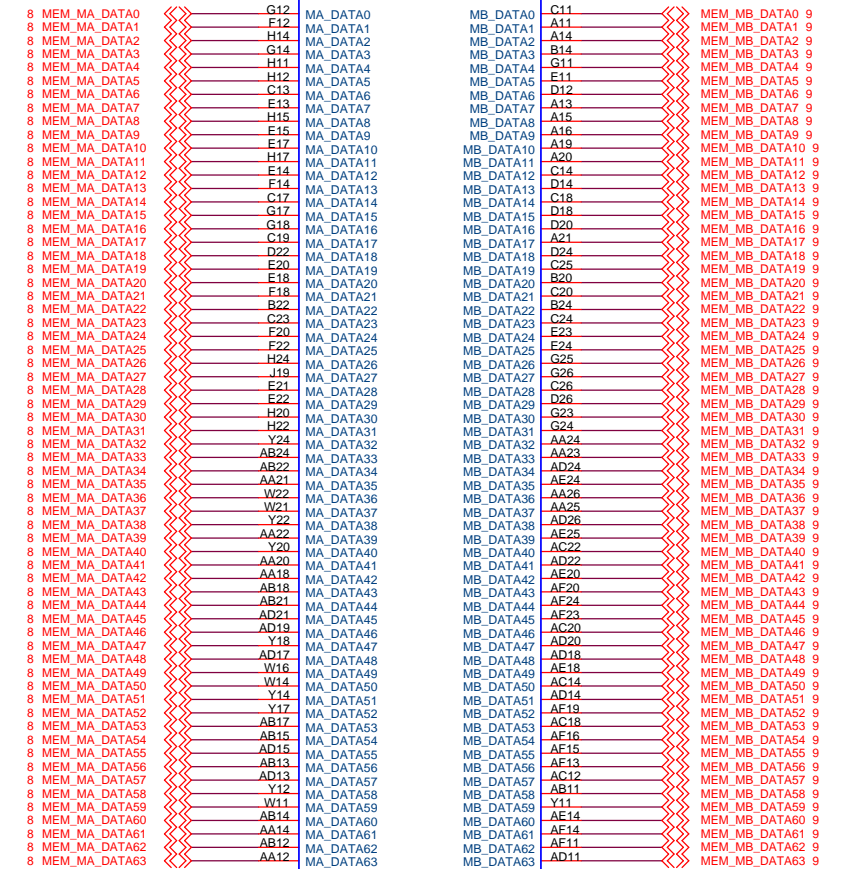
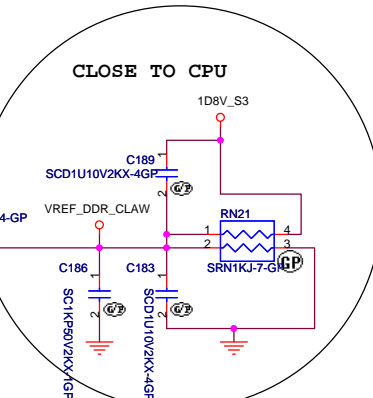
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>HISTORY</b>			
Size	Document Number		Rev
<b>A3</b>	<b>Cathedral Peak 2A</b>		<b>-1</b>
Date:	Friday, August 22, 2008		
		Sheet 2 of	43
		1	



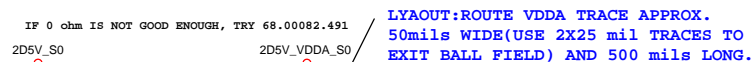




SKT-CPU638P-GP-U2

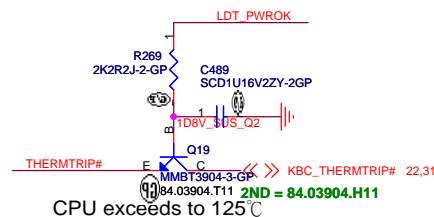
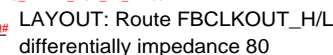


SKT-CPU638P-GP-U2



LYAOUT:ROUTE VDDA TRACE APPROX.  
50mils WIDE(USE 2X25 mil TRACES TO  
EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU



Title			
CPU Control&Debug (3/4)			
Size	Document Number	Rev	
A3	Cathedral Peak 2A	-1	
Date:	Friday, August 22, 2008	Sheet	6 of 43





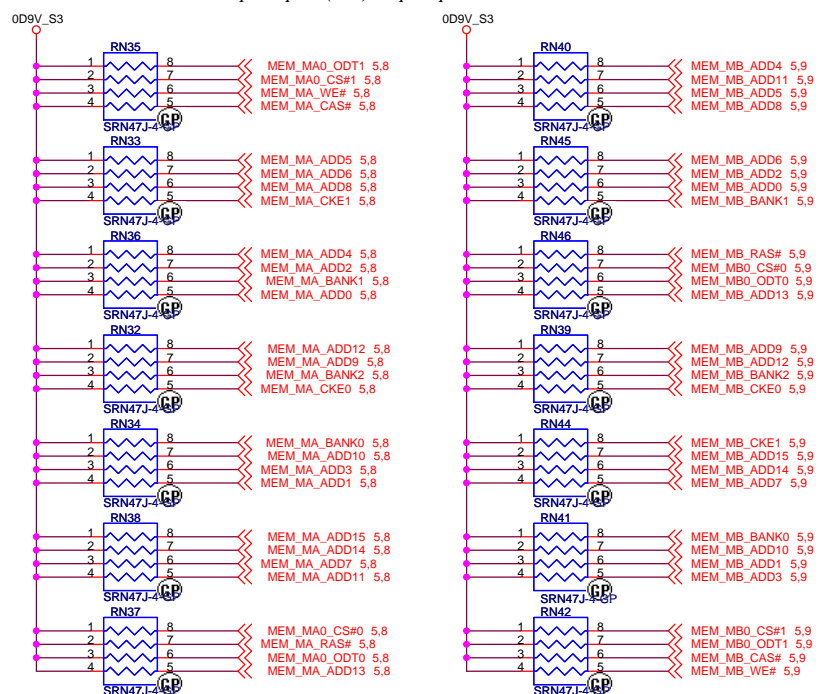






## PARALLEL TERMINATION

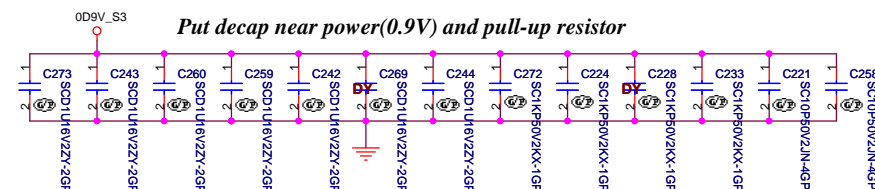
*Put decap near power(0.9V) and pull-up resistor*



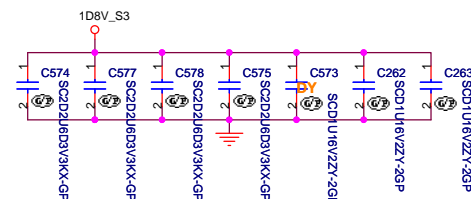
**Do not share the Term resistor between the DDR address and Control Signals.**

## Decoupling Capacitor

***Put decap near power(0.9V) and pull-up resistor***

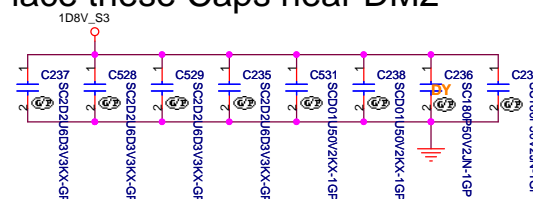


Place these Caps near DM1



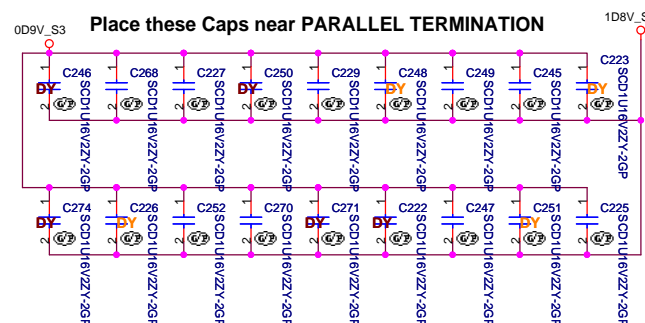
Layout Note:  
Place one cap close to every 2 pullup  
resistors terminated to 0D9V\_S3

Place these Caps near DM2



Layout Note:  
Place one cap close to every 2 pullup  
resistors terminated to 0D9V S3

**Place these Caps near PARALLEL TERMINATION**



<Core Design>

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Title
-------

## DDR DAMPING & TERMINATION

Size  
A:

Document Number

## Cathedral Peak 2A

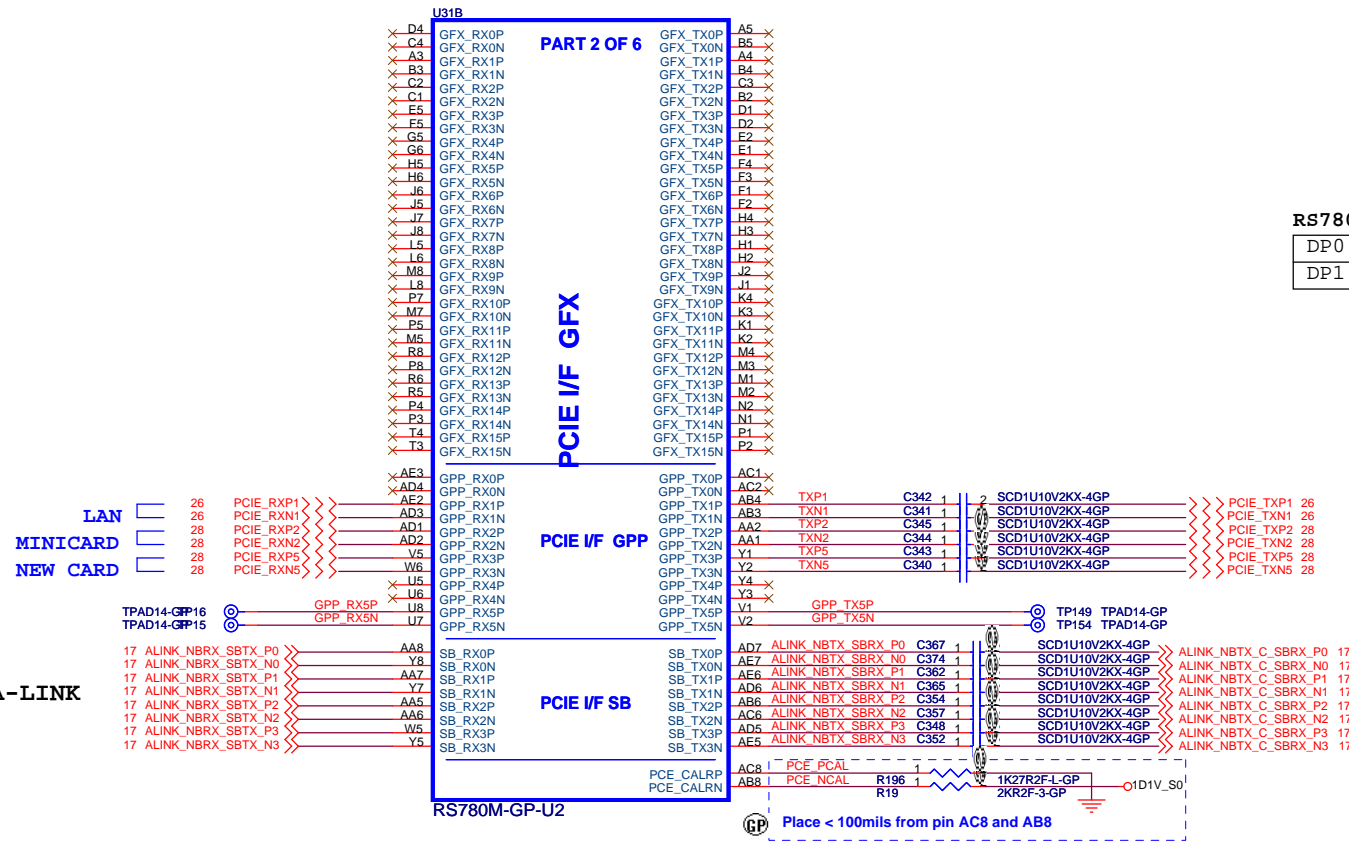
Rev

Date: Friday, August 22, 2008

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Placement: close RS780



RS780M Display Port Support(muxed on GFX)

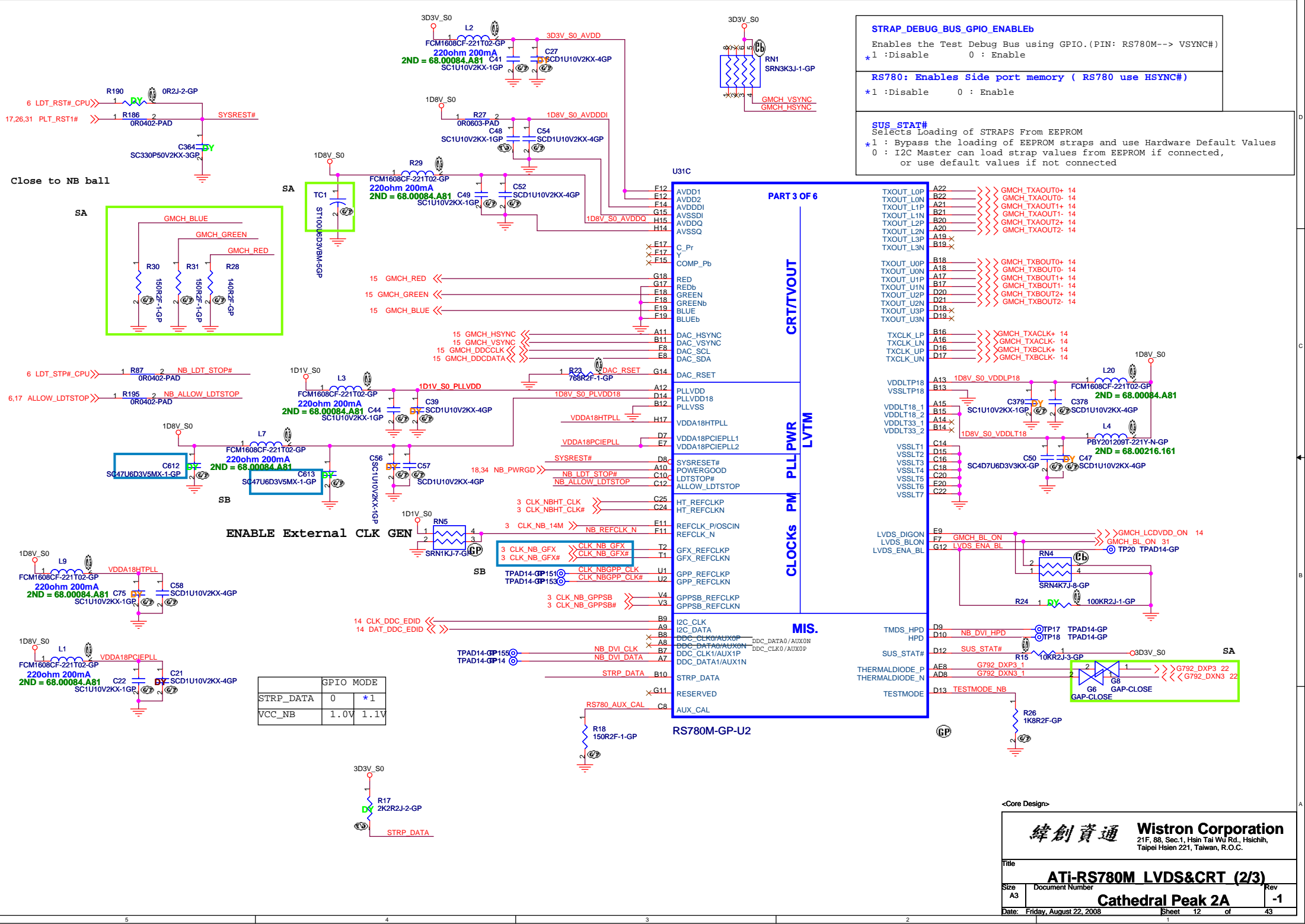
DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

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Taipei Hsien 221, Taiwan, R.O.C.

ATI-RS780M HT LINK&PCIE(1/3)  
Cathedral Peak 2A

Rev -1

Sheet 11 of 43

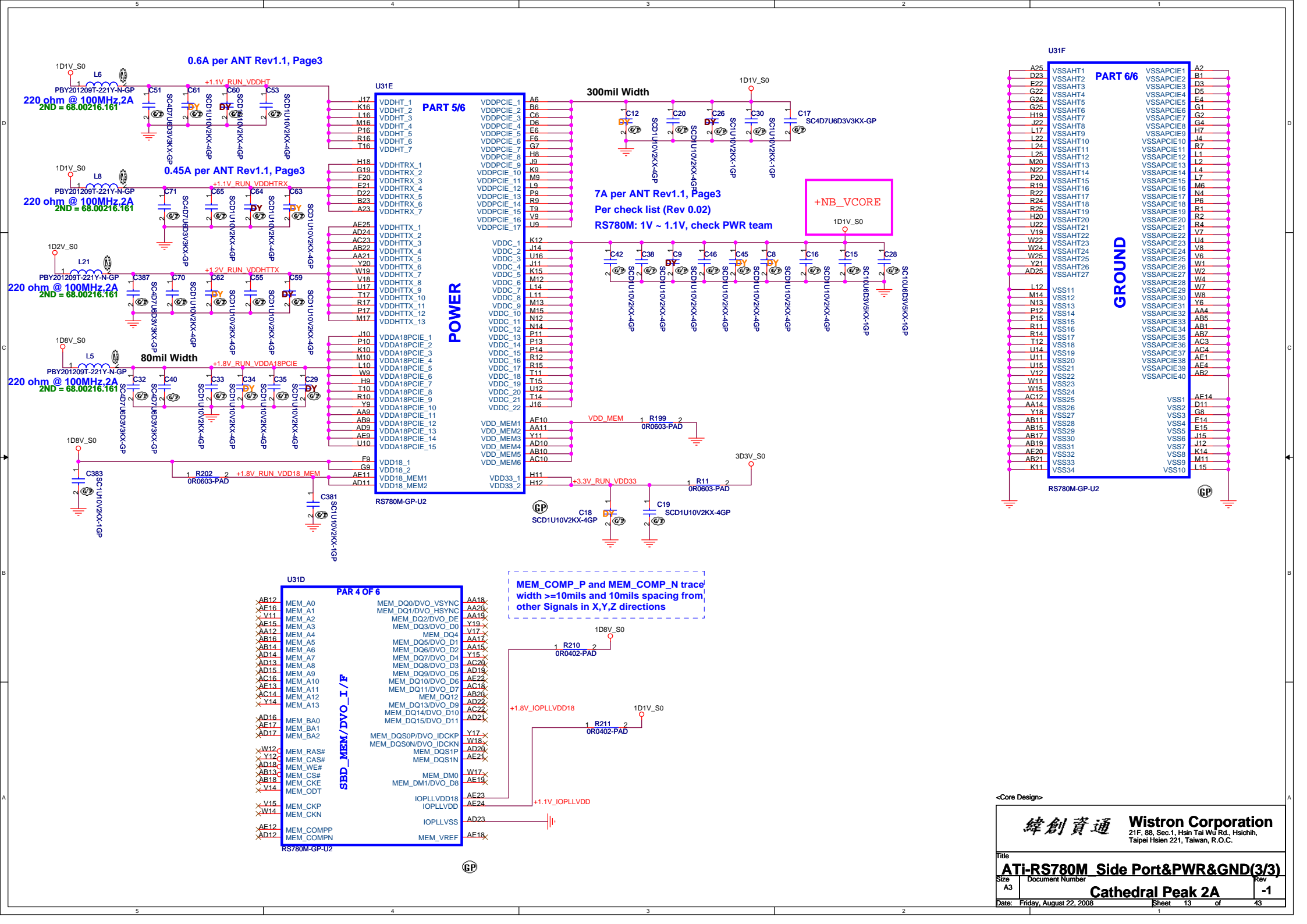


**STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb**  
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)  
\* 1 :Disable      0 : Enable

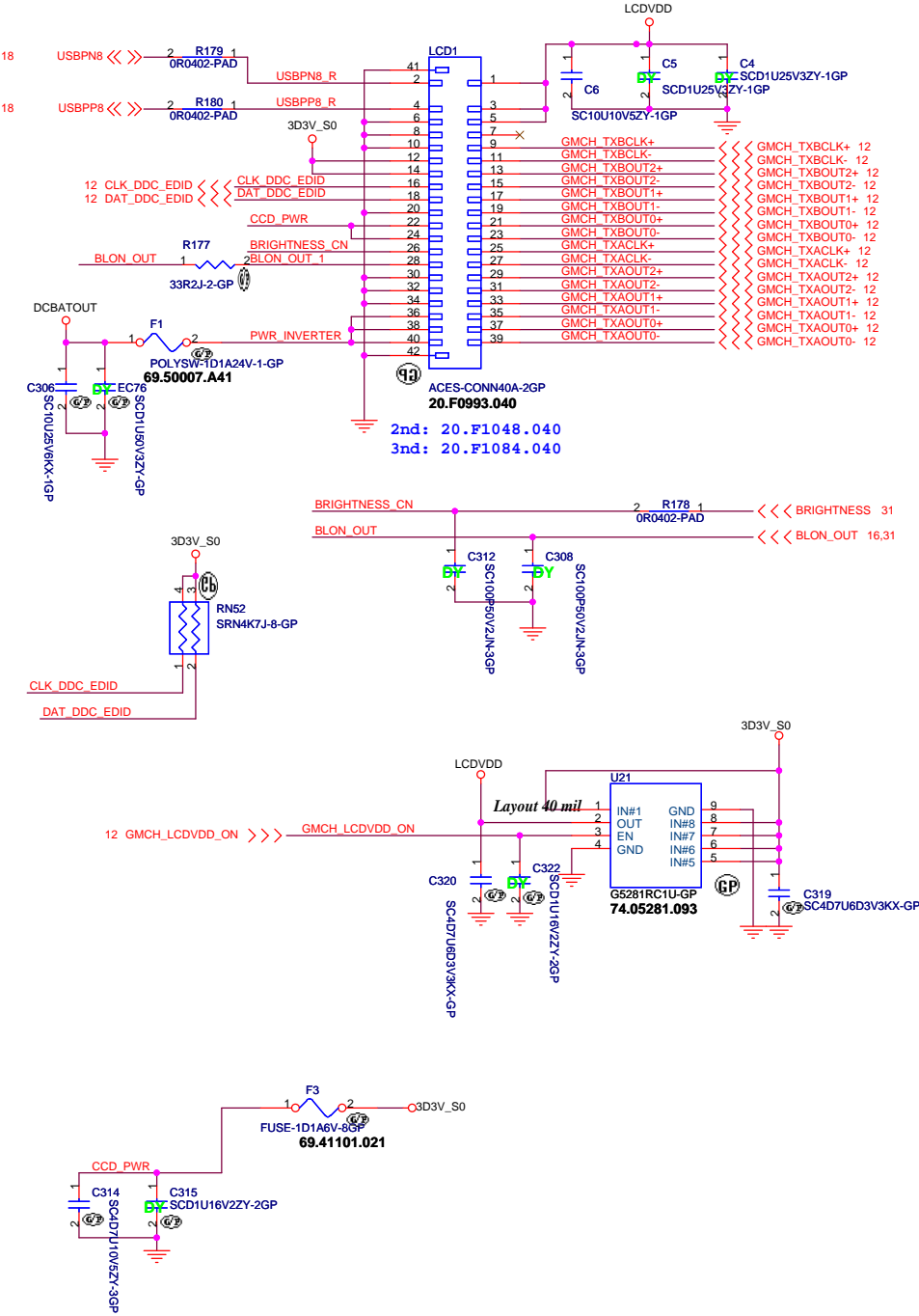
**RS780: Enables Side port memory ( RS780 use HSYNC#)**  
\* 1 :Disable      0 : Enable

**SUS\_STAT#**  
Selects Loading of STRAPS From EEPROM  
\* 1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected,  
or use default values if not connected

	GPIO MODE
STRP_DATA	0    * 1
VCC_NB	1.0V   1.1V



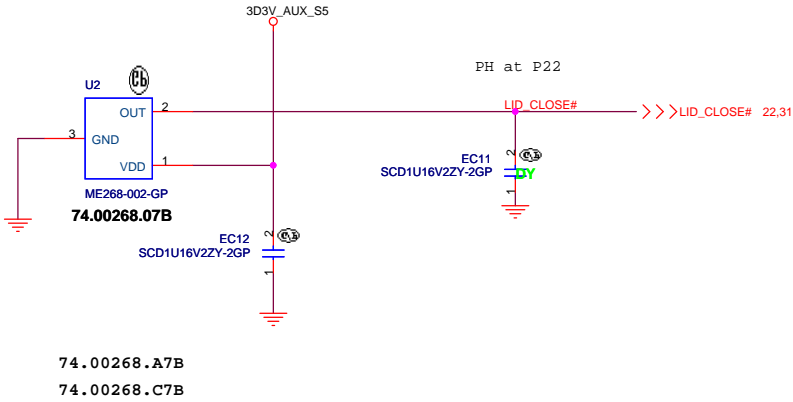
LCD/INVERTER/CCD CONN



Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

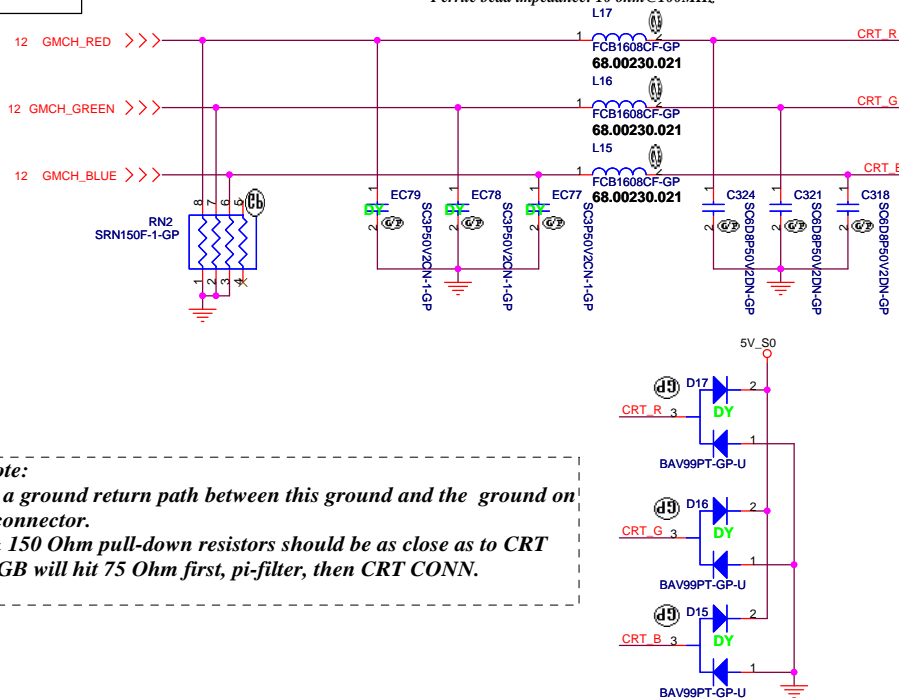
Cover Up Switch



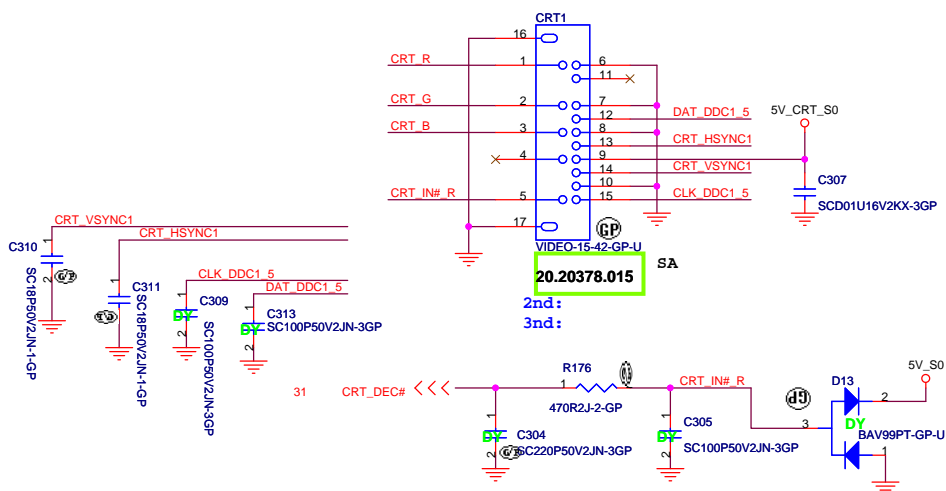


Layout Note:  
Place these resistors  
close to the CRT-out  
connector

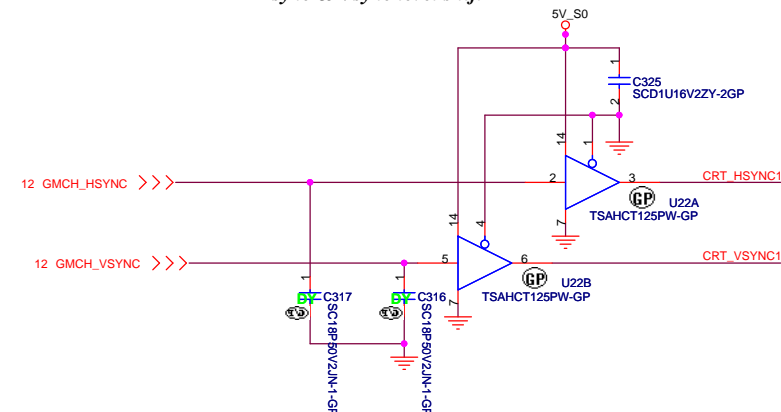
Ferrite bead impedance: 10 ohm@100MHz



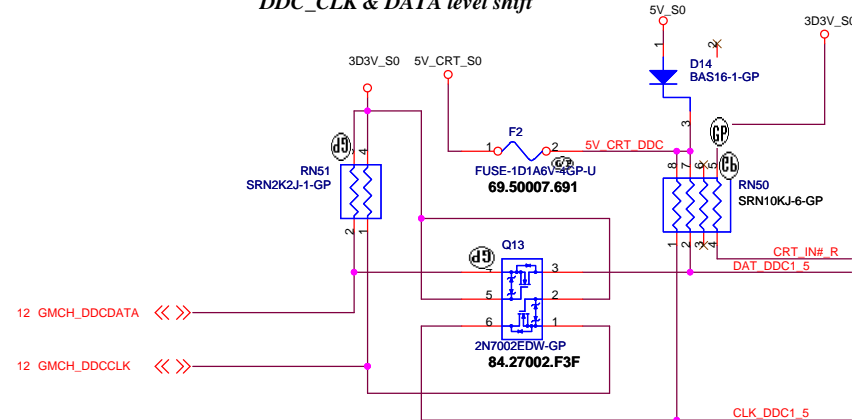
## CRT I/F & CONNECTOR



## Hsync & Vsync level shift



## DDC\_CLK & DATA level shift



<Core Design>

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Title		
CRT Connector		
Size	Document Number	Rev
Cathedral Peak 2A		-1
Date: Friday, August 22, 2008	Sheet 15 of 43	

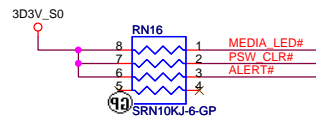
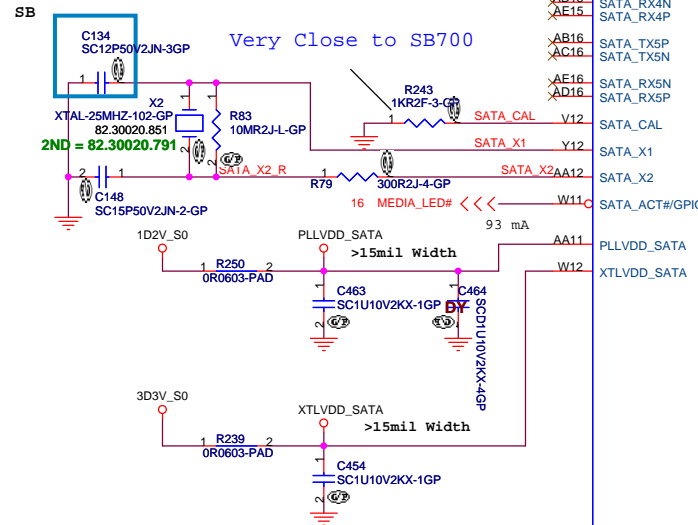
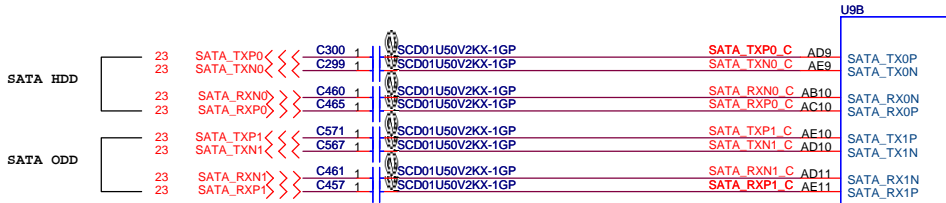








PLACE SATA AC DECOUPLING  
CAPS CLOSE TO SB700



## SB700

Part 2 of 5

SERIAL ATA

SATA PWR

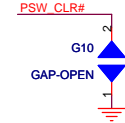
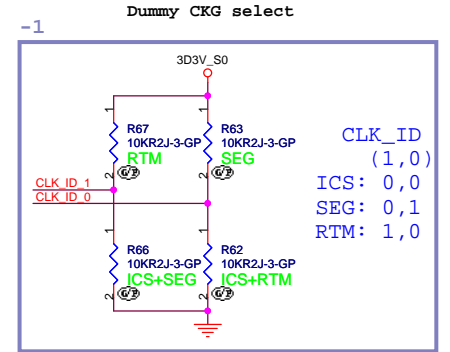
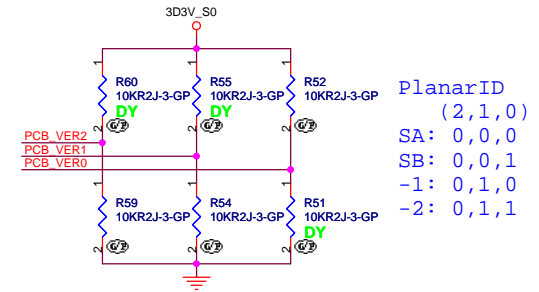
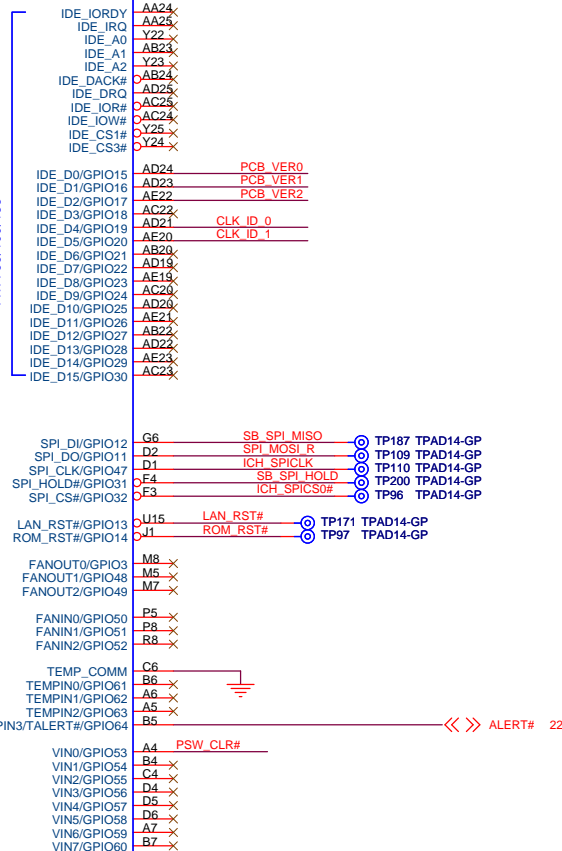
HW MONITOR

ATA 68/100/133

SPI ROM

HW MONITOR

SB700-1-GP-U1



<Core Design>

緯創資通 Wistron Corporation

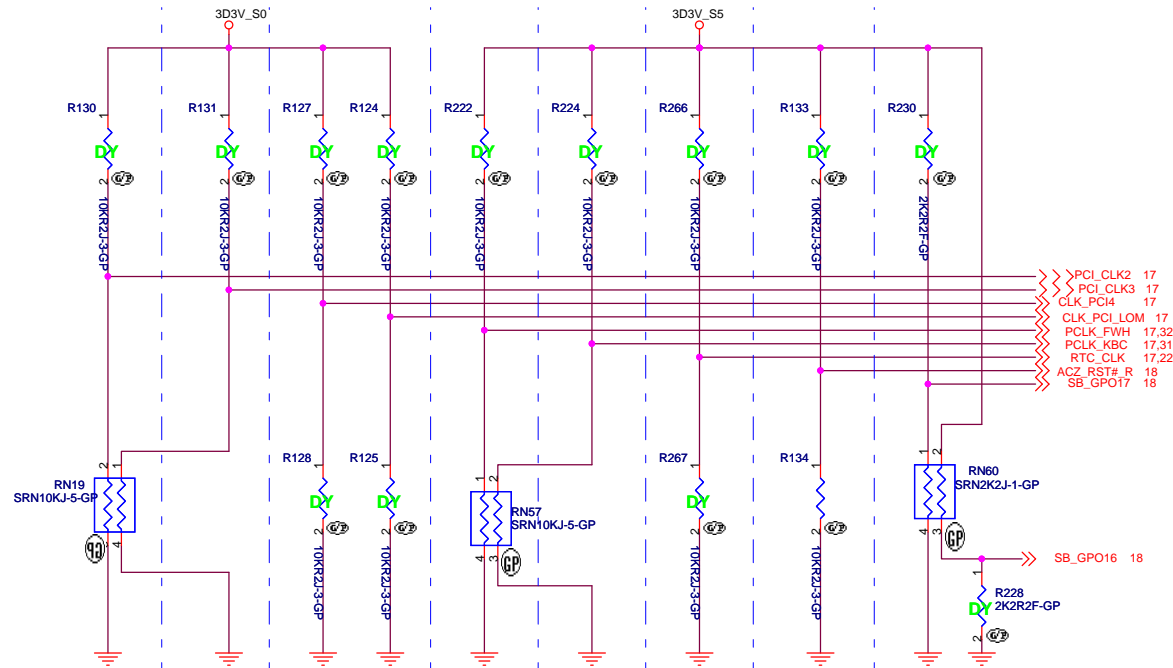
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title			ATi-SB700 SATA-IDE (3/5)
Size	Document Number	Rev	
A3			
Date: Friday, August 22, 2008			Sheet 19 of 43
Cathedral Peak 2A			-1

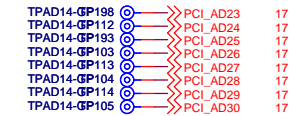


## REQUIRED STRAPS

### REQUIRED SYSTEM STRAPS



## DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

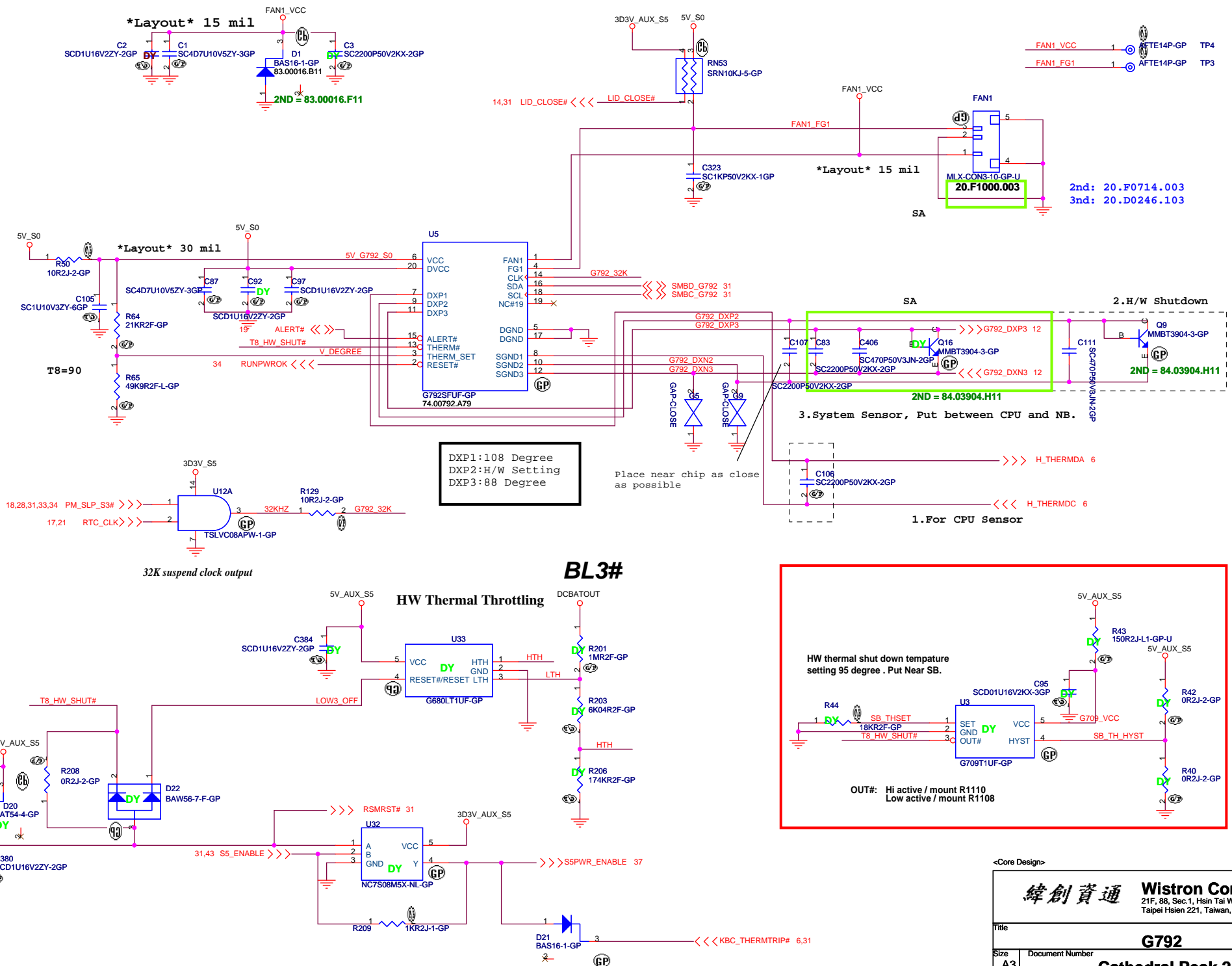
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI\_AD[30:23]

<Core Design>

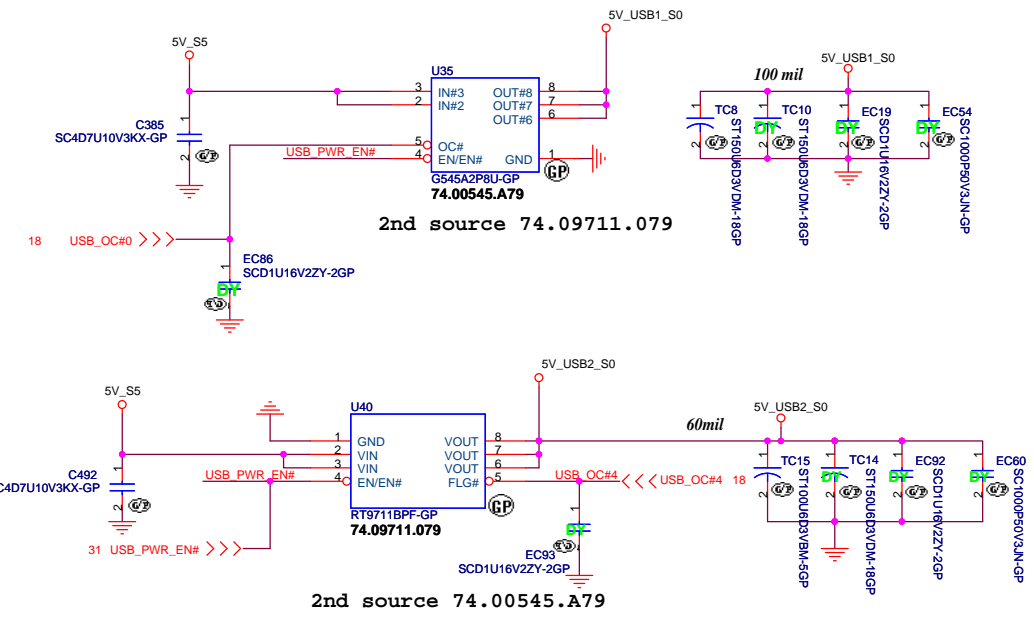
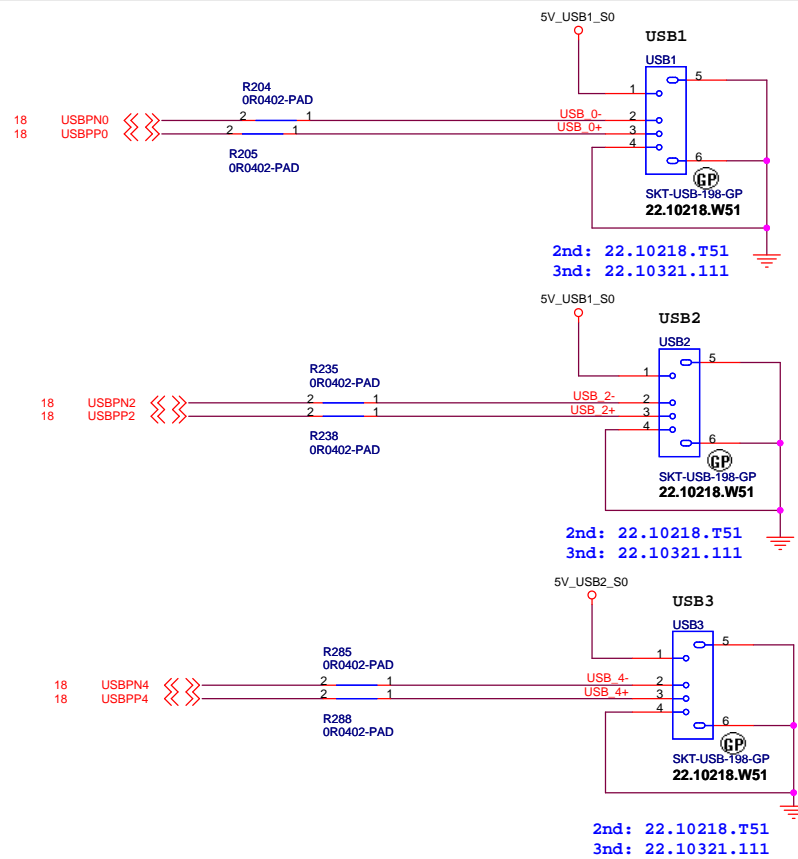
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		ATi-SB700 STRAPPING (5/5)	
Size	Document Number	Rev	
A3		Cathedral Peak 2A	
Date:	Friday, August 22, 2008	Sheet	21 of 43



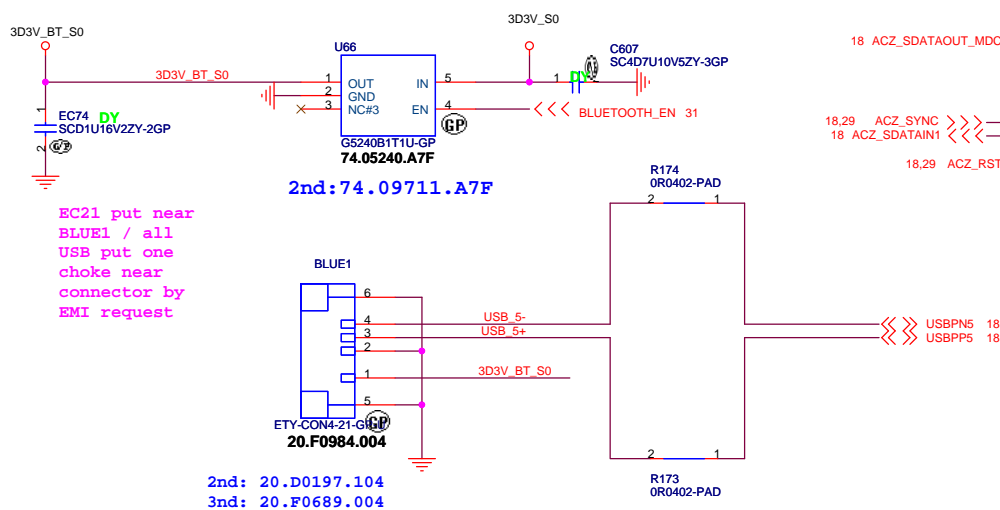




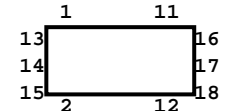
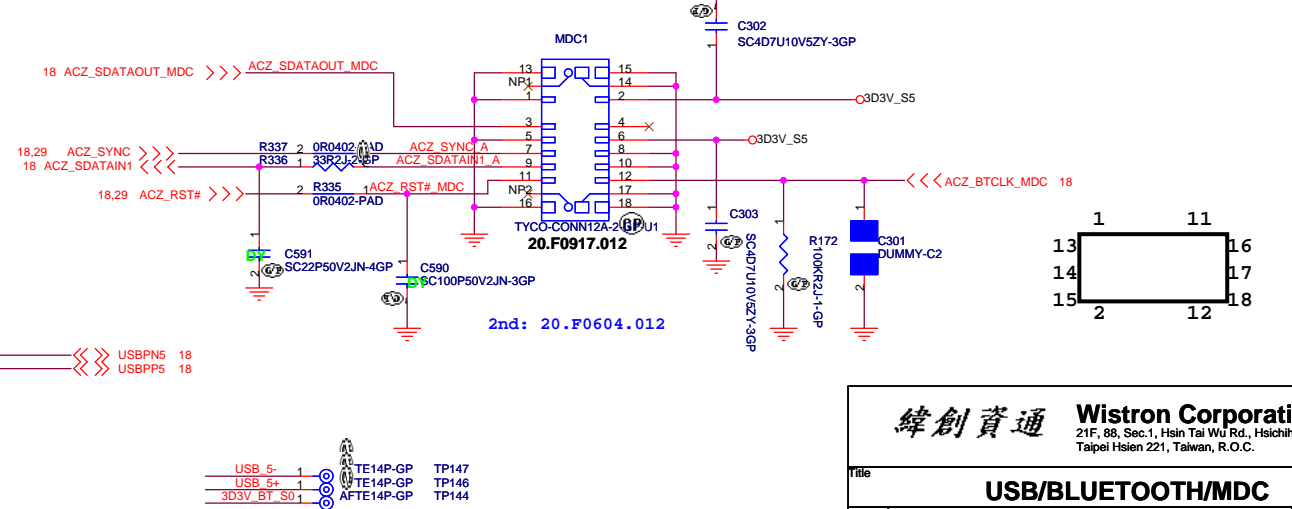


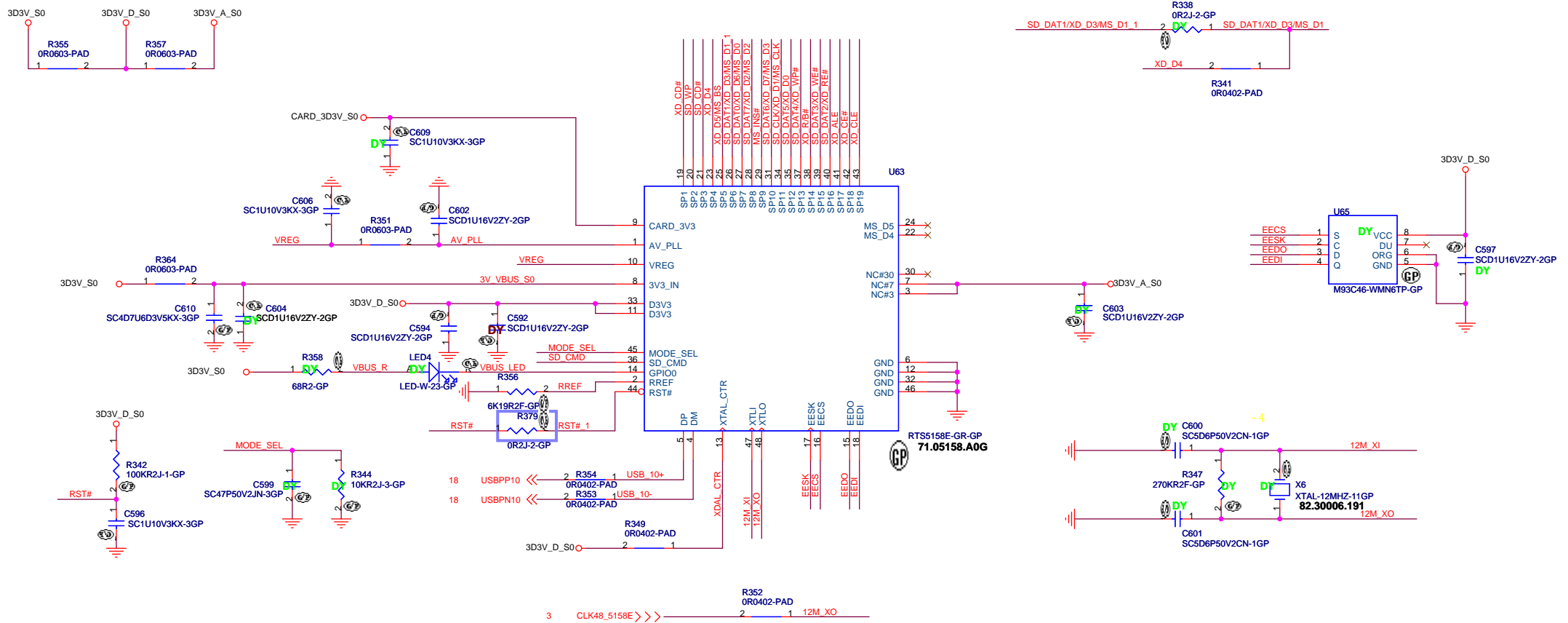
## BLUETOOTH MODULE

1.5A / High Active Voltage 2V

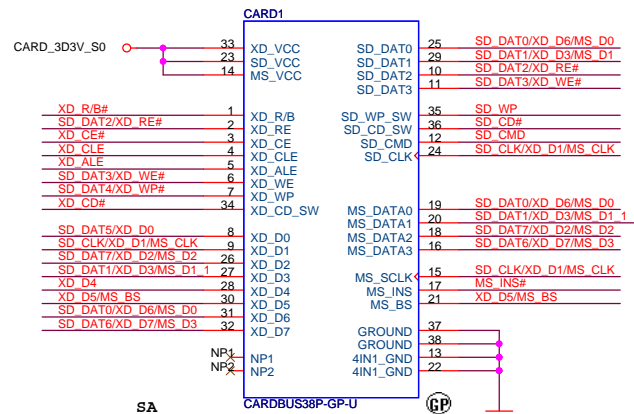
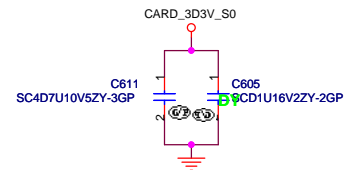


## MDC 1.5 CONN



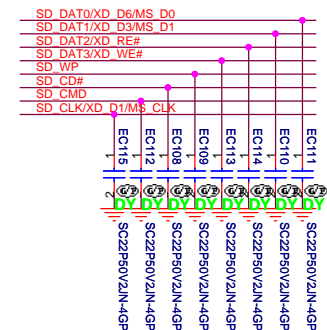


## 5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



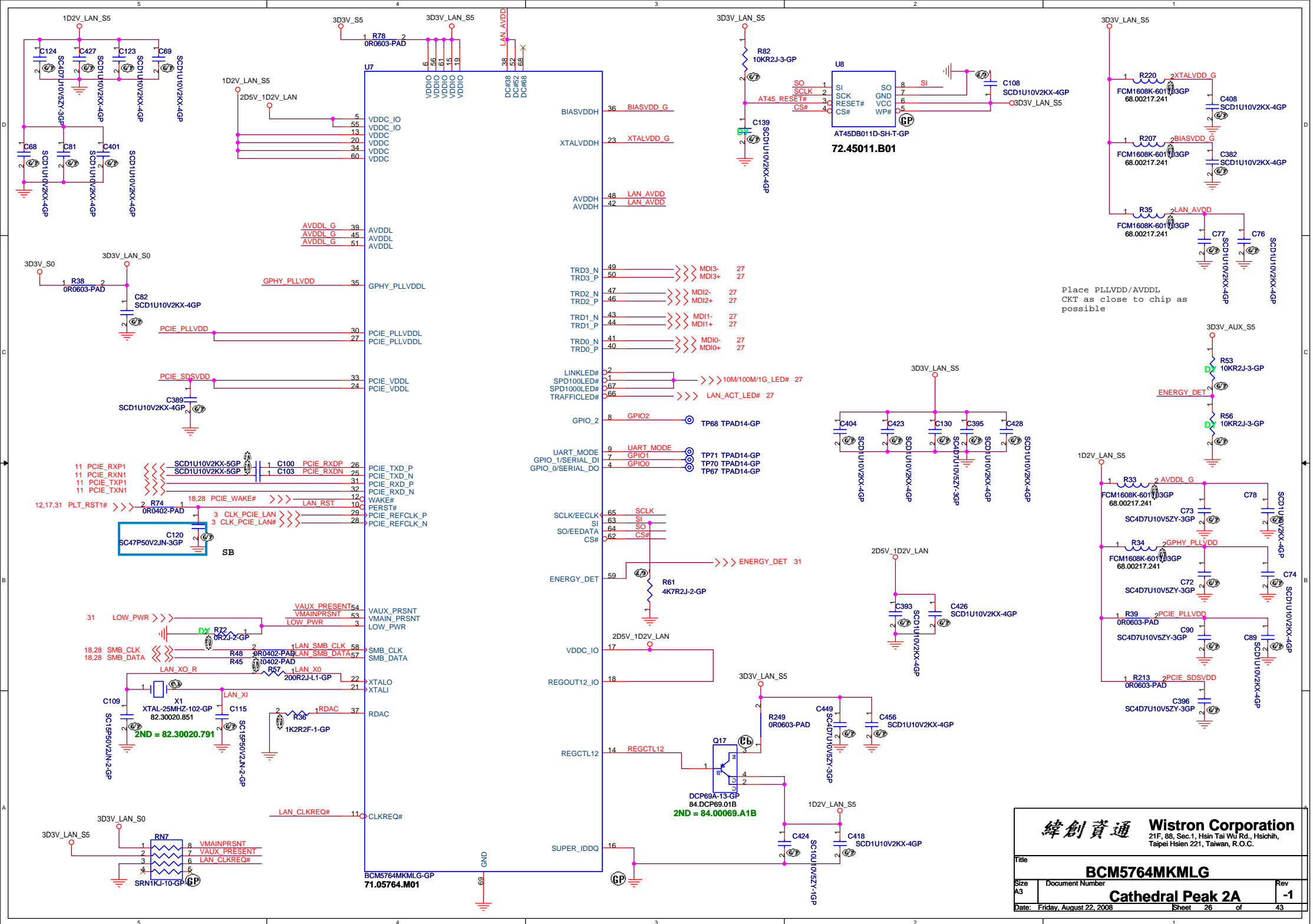
2nd:20.I0081.001  
3rd:20.I0067.001

20.I0079.001



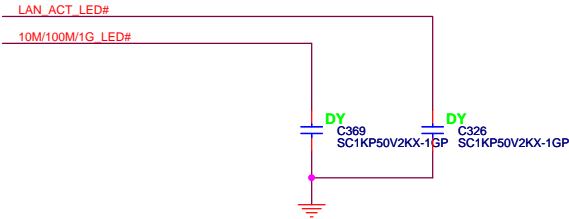
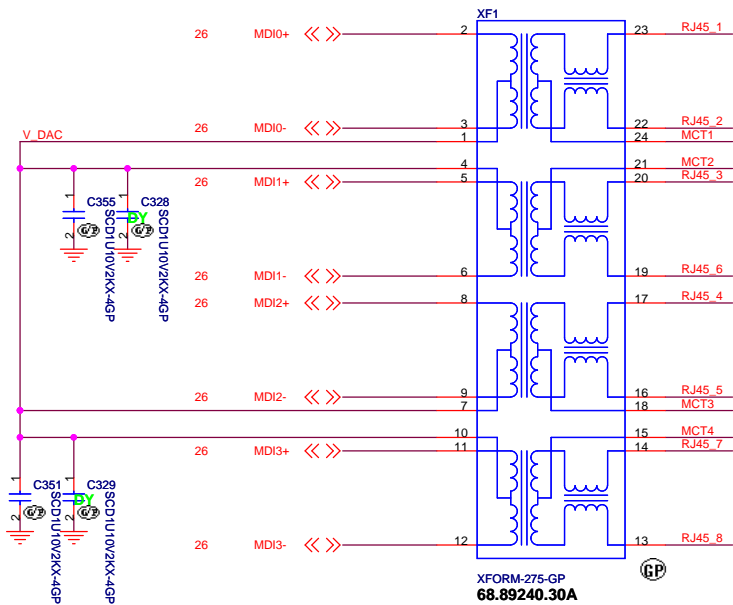
**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	CARDREADER- RTS5158E		
Size	Document Number		Rev
		Cathedral Peak 2A	-1
Date: Friday, August 22, 2008	Sheet	25	of 43

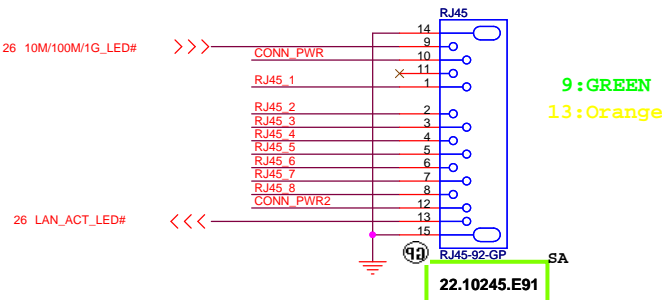


# LAN Connector

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

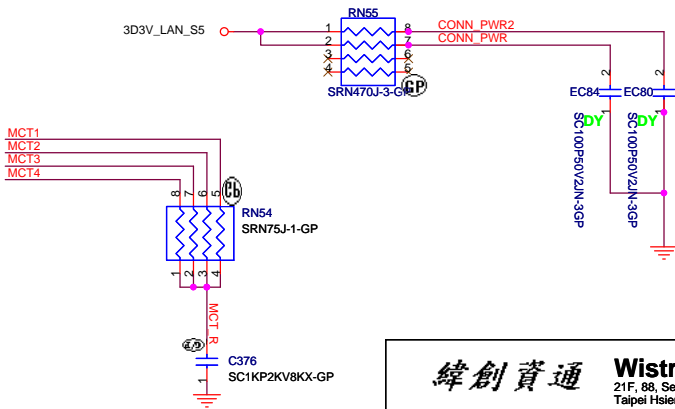


# LAN Connector



2nd:  
LAN Link: Green(9), behavior is the same for 10/100/1000 bits  
LAN Data: Yellow(13), when LAN is transferring data.

DOC\_TIP,DOC\_RING,TIP,RING:  
W/S : 10/100 @ Surface layers  
10/20 @ Inner layers



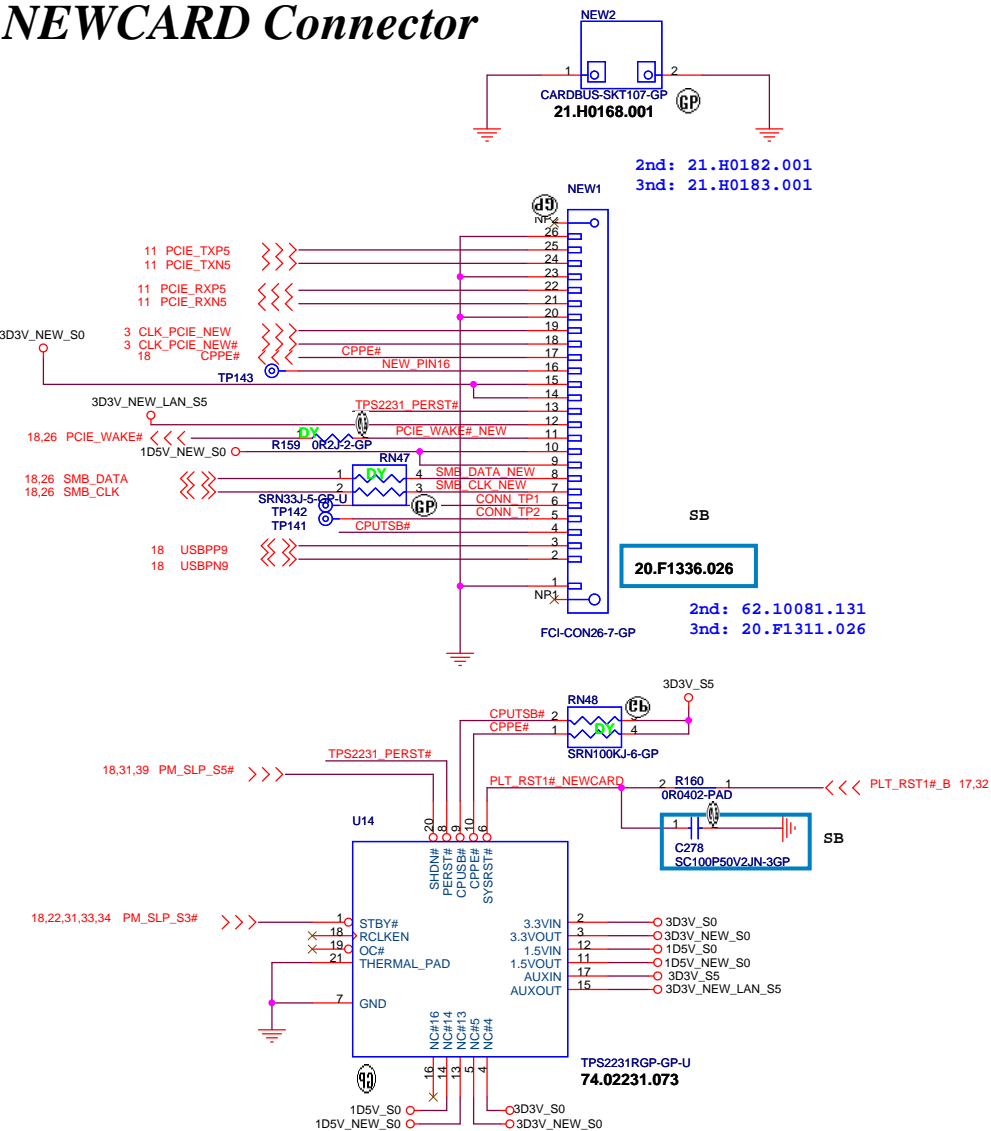
緯創資通

Wistron Corporation

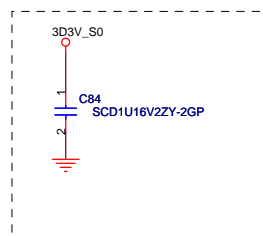
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
LAN CONN		
Size	Document Number	Rev
A3		-1
Date:	Friday, August 22, 2008	Sheet 27 of 43

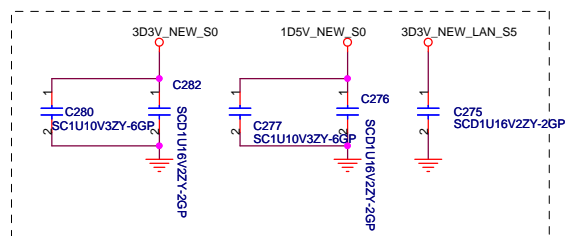
## ***NEWCARD Connector***



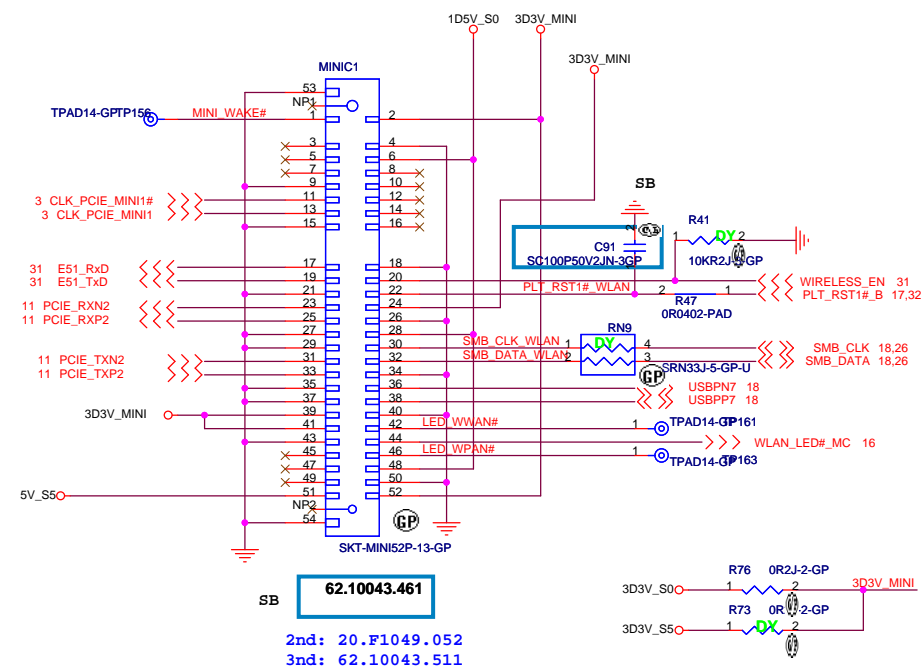
Place them Near to Chip



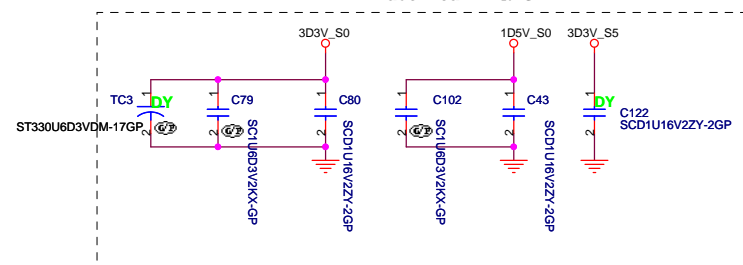
Place them Near to Connector

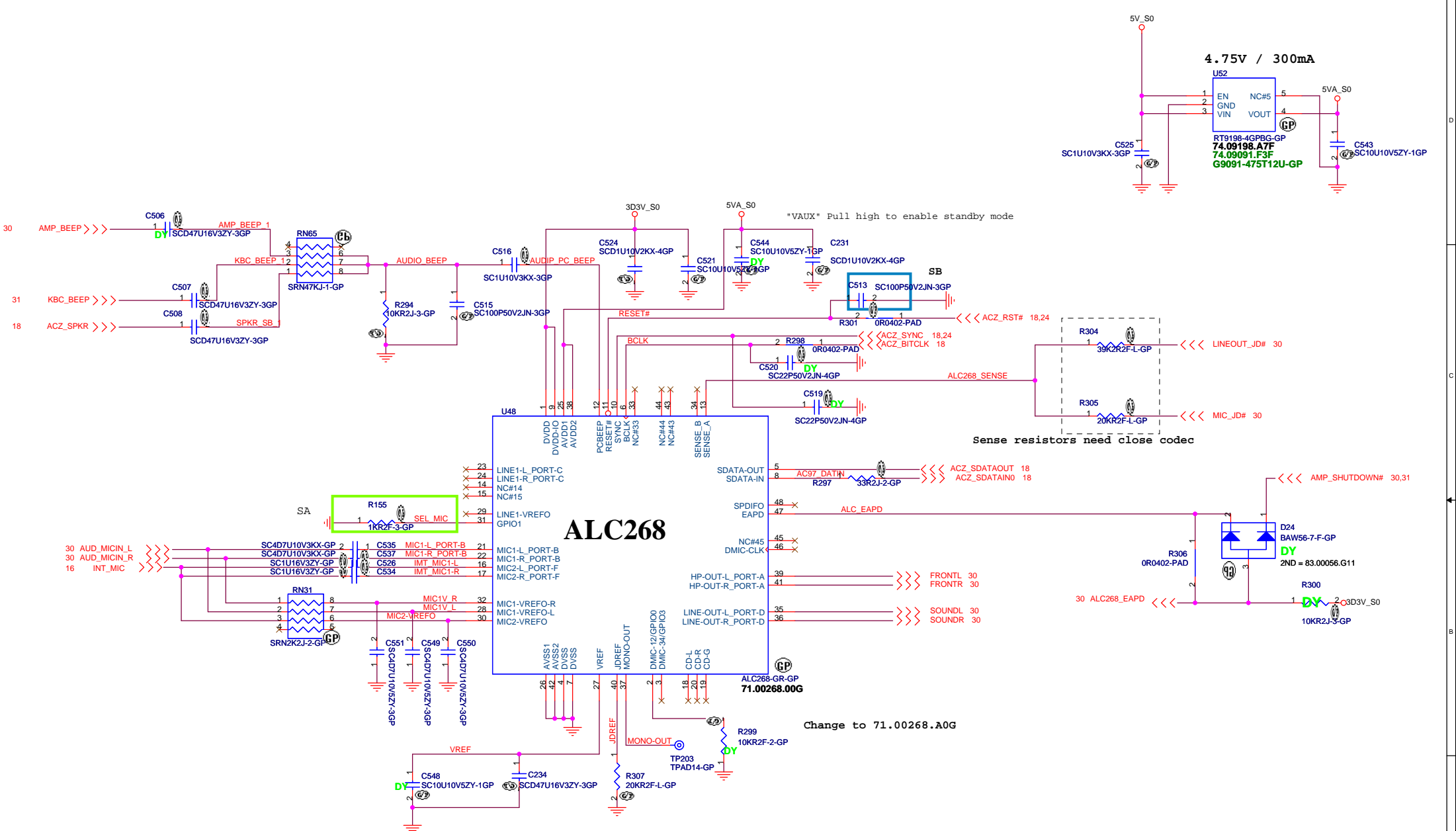


### *Mini Card Connector(WLAN)*



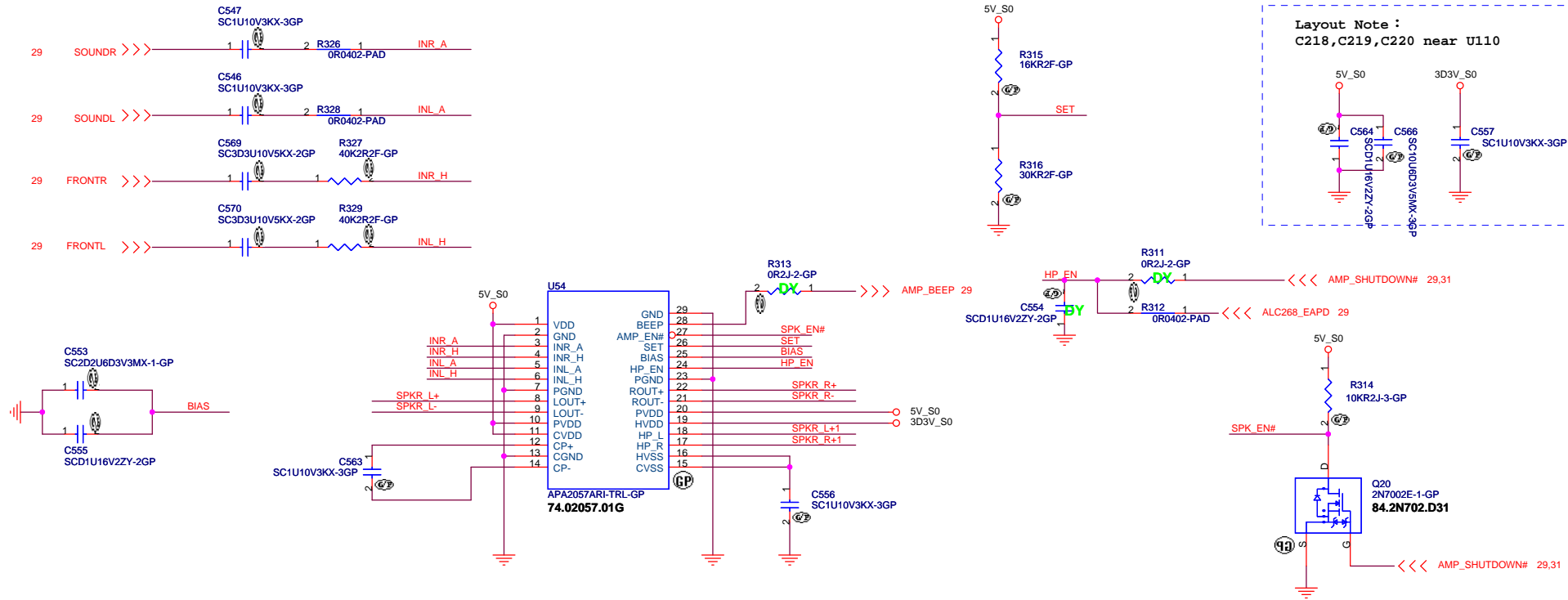
Place near MINIC1



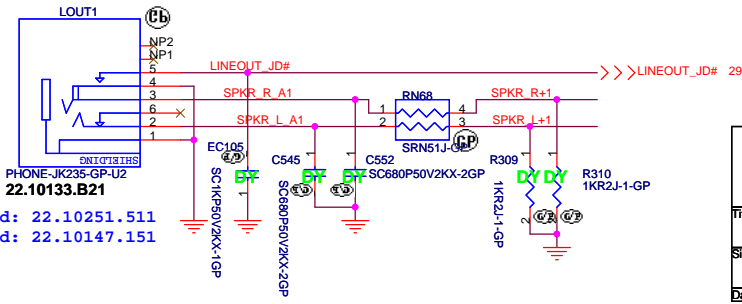




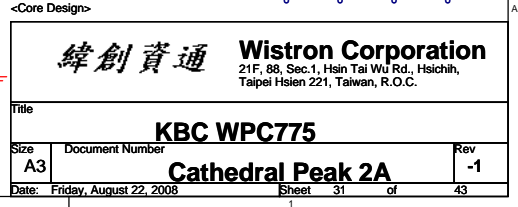
# AUDIO OP AMPLIFIER



## LINE OUT

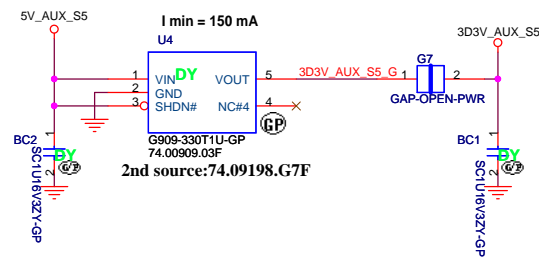


<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>AUDIO AMP AND JACK</b>	
Title Size Date: Friday, August 22, 2008	Document Number <b>Dolomites</b> Sheet 30 of 43
Rev <b>-1</b>	

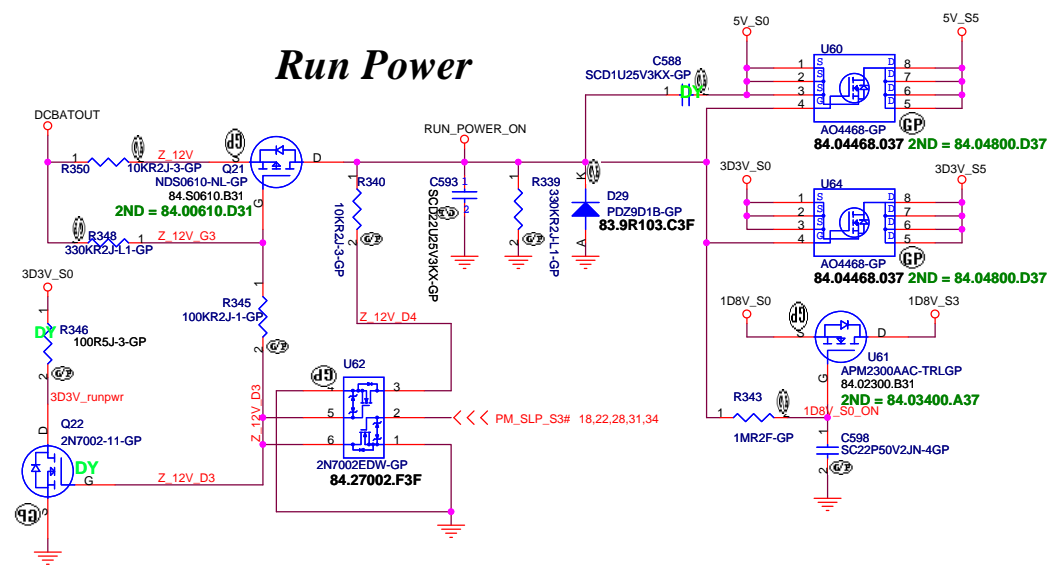




Aux Power 3D3V\_AUX\_S5

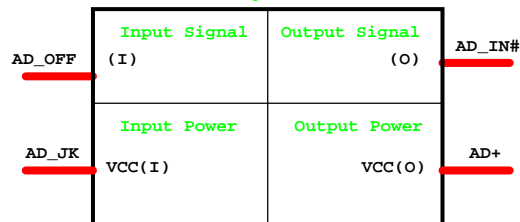


Run Power

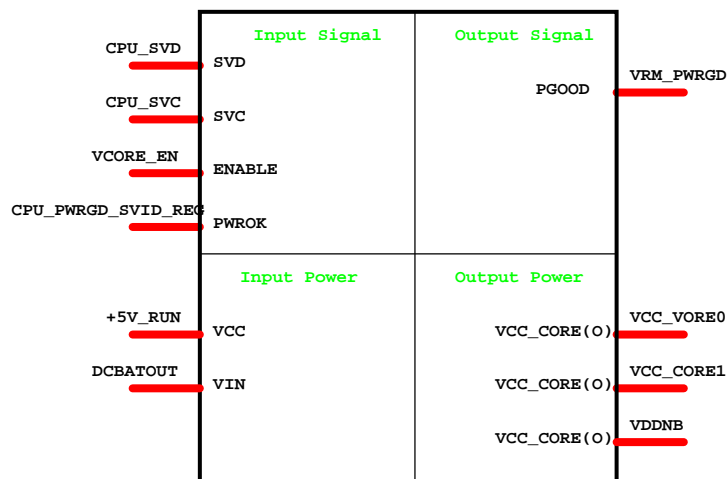




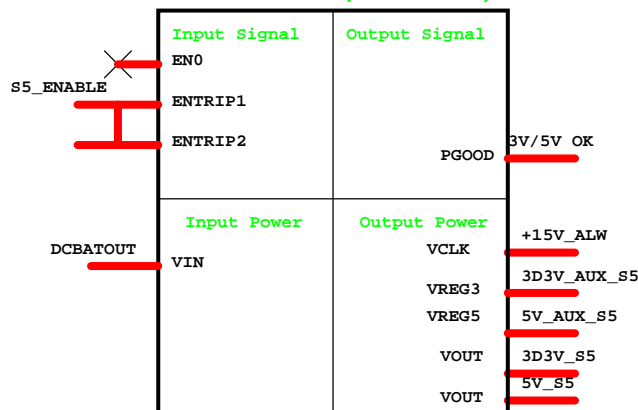
## Adapter



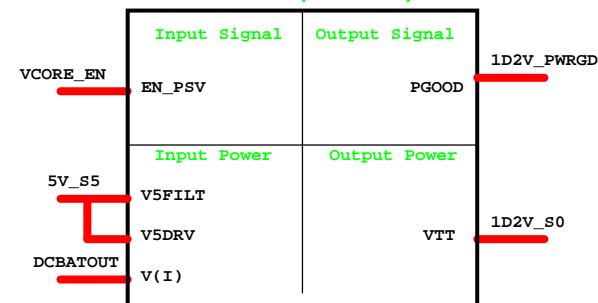
## CPU\_CORE ISL6265HRTZ



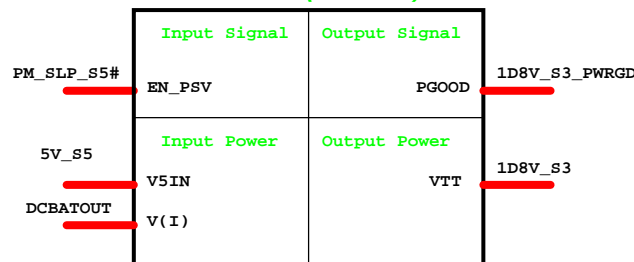
## DCDC 5V/3D3V(TPS51125)



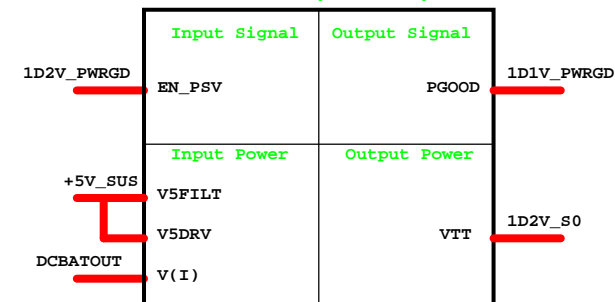
## DCDC 1D2V(RT8202)



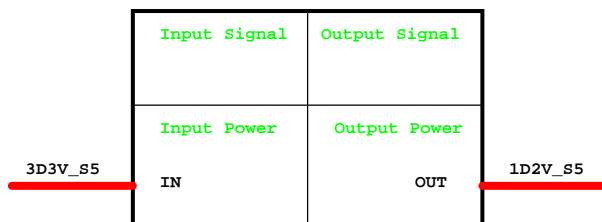
## DCDC 1D8V(RT8202)



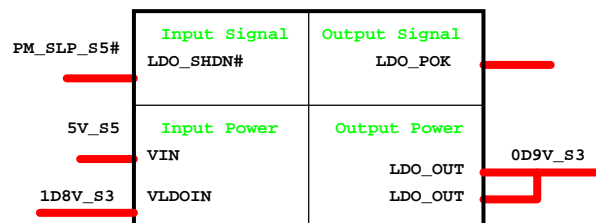
## DCDC 1D1V(RT8202)



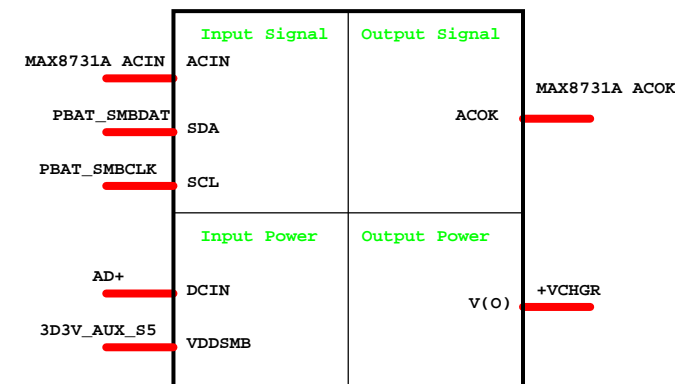
## 1D2V LDO G9161



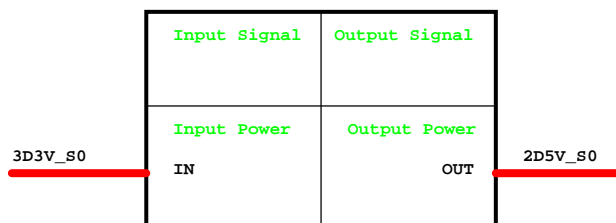
## 0D9V LDO RT9026



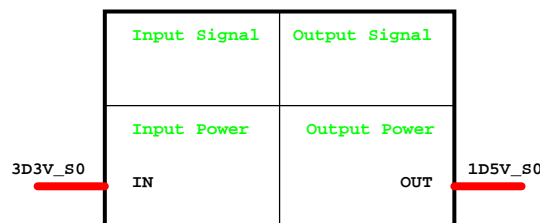
## CHARGER MAX8731



## 2D5V LDO R9161



## 1D5V LDO G9571



<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

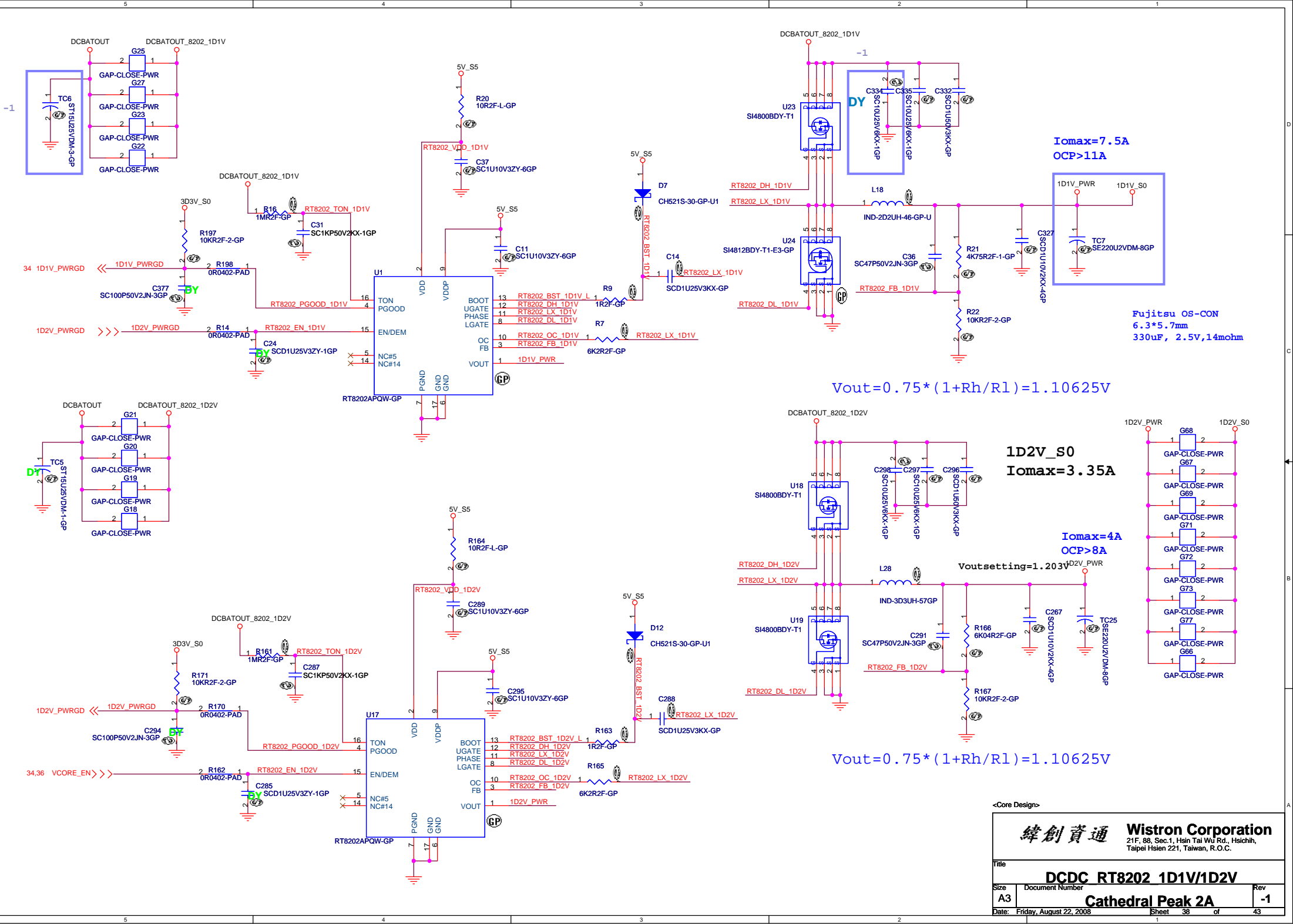
Title			Power Block Diagram
Size	Document Number	Rev	
A3		-1	
Date:	Friday, August 22, 2008	Sheet	35 of 43

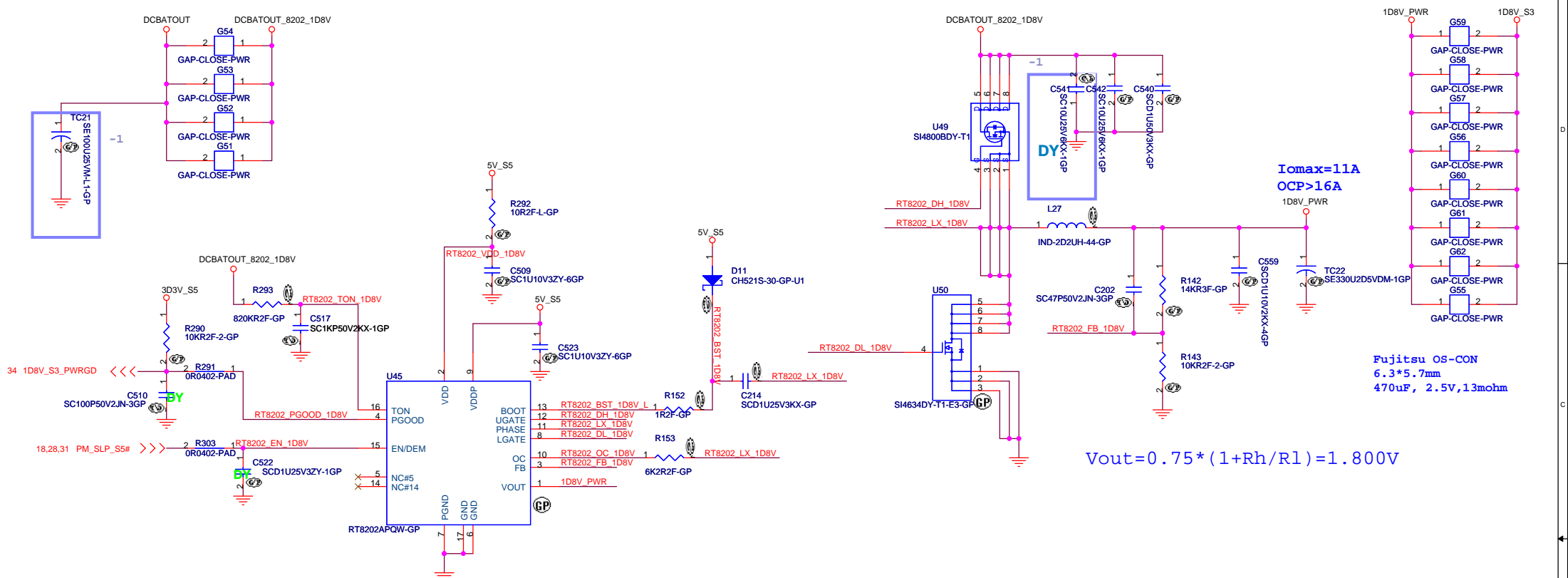
Cathedral Peak 2A





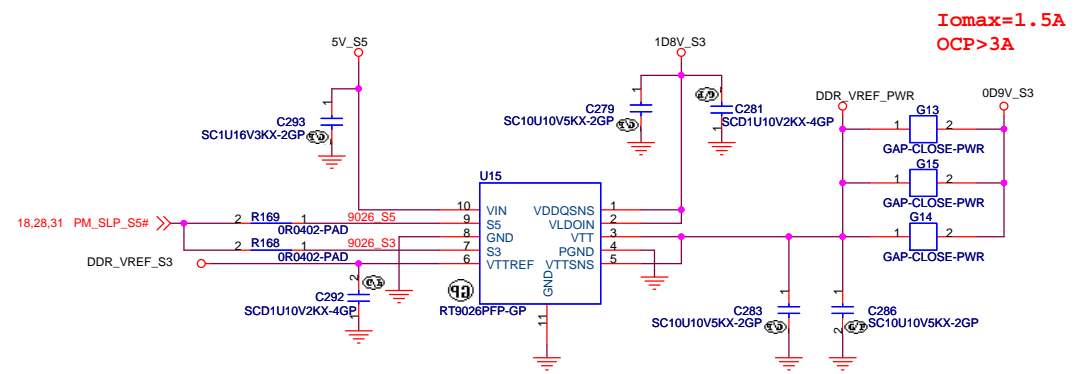


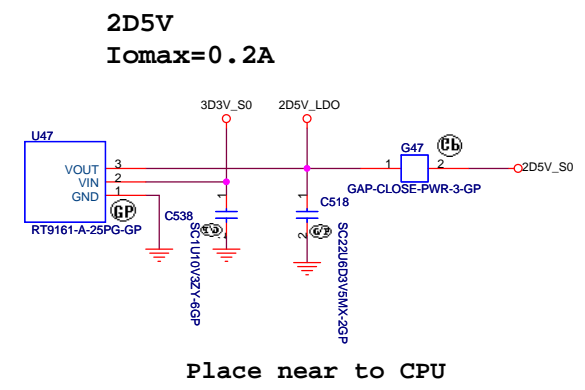
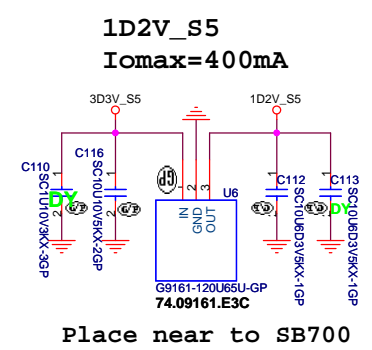
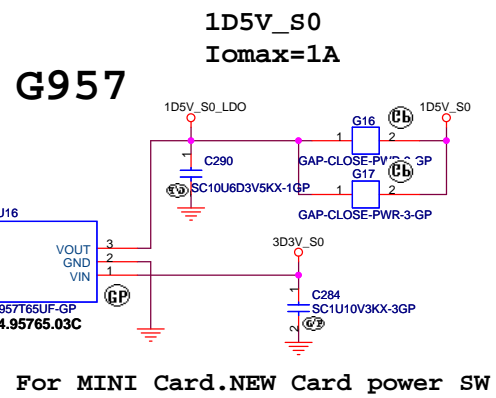


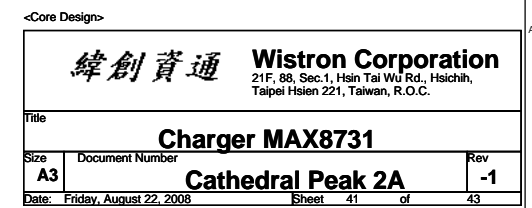


$$V_{out} = 0.75 * (1 + R_h / R_l) = 1.800V$$

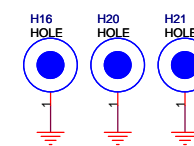
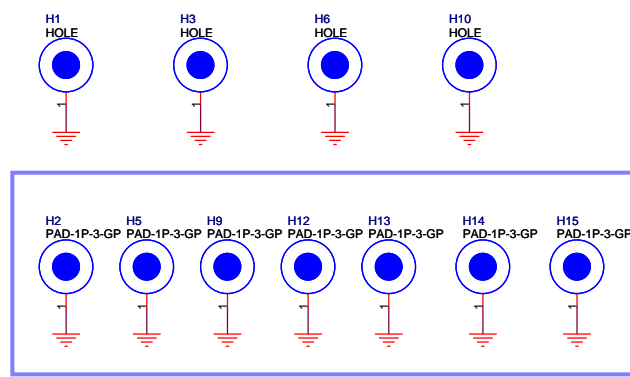
## DDR\_0.9V



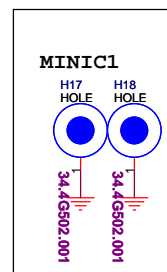
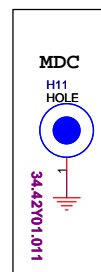
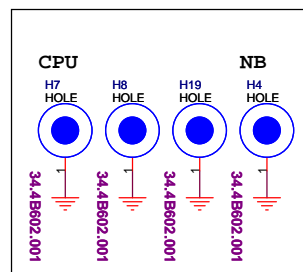
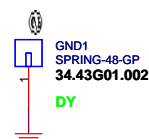








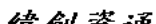
**BOTTOM**



-1

Signal	Pin	Connector	Function
3D3V_S0	TP140	TPAD14-GP	
3D3V_AUX_S5	TP148	TPAD14-GP	
3D3V_S5	TP145	TPAD14-GP	
5V_S5	TP127	TPAD14-GP	
18,31 PM_PWRBTN#	TP65	TPAD14-GP	
6,17 CPU_PWRGD	TP188	TPAD14-GP	
22,31 S5_ENABLE	TP160	TPAD14-GP	
6,17 CPU_LDT_RST#	TP77	TPAD14-GP	

**Test Point**放在Dimm Door打開可量測處

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>EMI/Spring/Boss</b>			
Size	Document Number	<b>Cathedral Peak 2A</b>	
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		Rev -1	